



5NN50-SE1

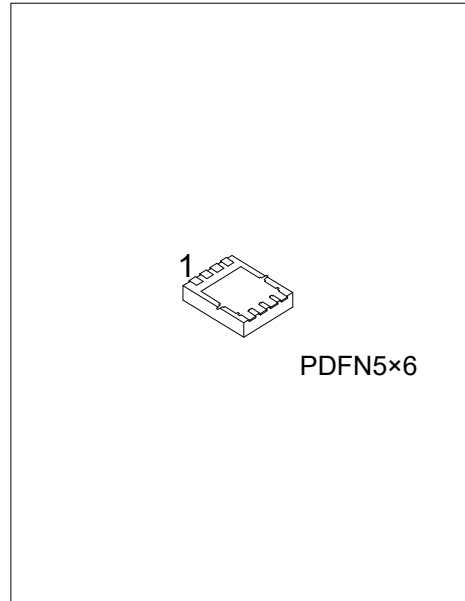
Preliminary

Power MOSFET

5.0A, 500V DUAL N-CHANNEL ENHANCEMENT MODE POWER MOSFET

■ DESCRIPTION

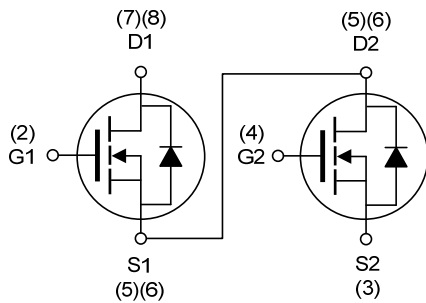
The UTC **5NN50-SE1** is a dual N-Channel enhancement mode silicon gate power MOSFET with Fast Body Diode, is designed high voltage, high speed power switching applications such, is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and have a high rugged avalanche characteristics. This power MOSFET is usually used at high speed switching applications in power supplies, PWM motor controls, high efficient AC to DC converters and bridge circuits.



■ FEATURES

- * $R_{DS(ON)} \leq 3.1 \Omega @ V_{GS}=10V, I_D=1.5A$
- * Fast body diode MOSFET technology
- * Fast Switching Speed
- * Simple Drive Requirement

■ SYMBOL



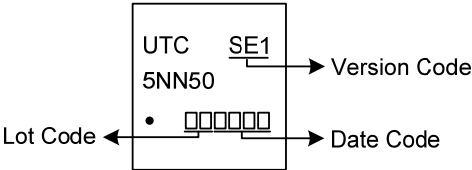
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
5NN50L-SE1-P5060-R	5NN50G-SE1-P5060-R	PDFN5×6	NC	G1	S2	G2	D2/ S1	D2/ S1	D1	D1	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>5NN50G-SE1-P5060-R</p>	<ul style="list-style-type: none"> (1)Packing Type (2)Package Type (3)Version Code (4)Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) P5060: PDFN5×6 (3) Version SE1 (4) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	5	A
	Pulsed (Note 2)	I_{DM}	10	A
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.2	V/ns
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	38	mJ
Power Dissipation		P_D	20	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 10\text{mH}$, $I_{AS} = 2.8\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.

4. $I_{SD} \leq 5.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	65	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	6.25	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

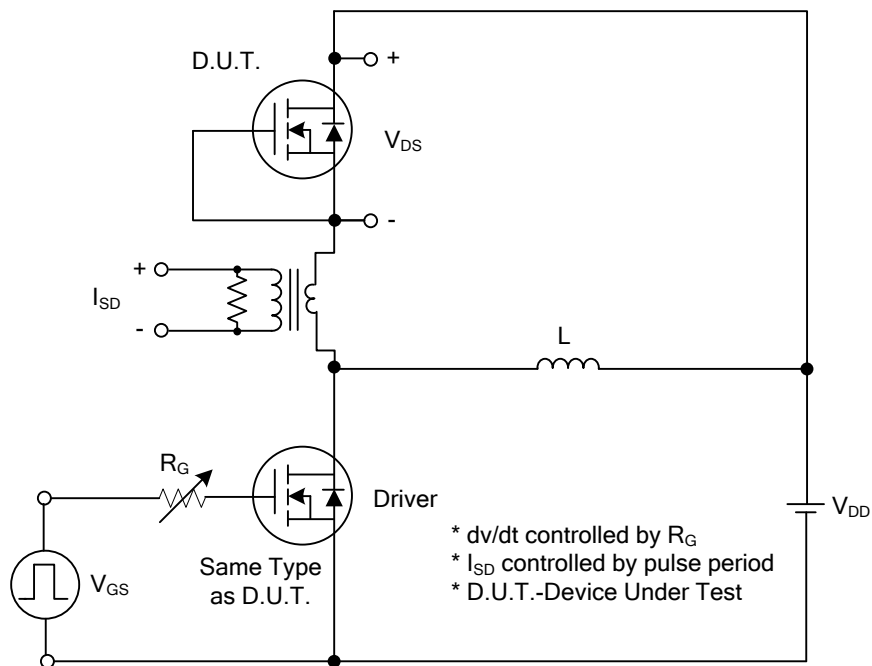
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	500			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$			10	μA
Gate-Source Leakage Current	Forward	I_{GSS}			100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=1.5\text{A}$			3.1	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=25\text{V}$, $f=1.0\text{MHz}$		253		pF
Output Capacitance	C_{OSS}			37		pF
Reverse Transfer Capacitance	C_{RSS}			3		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge (Note 1)	Q_G	$V_{DS}=50\text{V}$, $V_{GS}=10\text{V}$, $I_D=2.5\text{A}$ (Note 1, 2)		12		nC
Gate-source Charge	Q_{GS}			4		nC
Gate-Drain Charge	Q_{GD}			2		nC
Turn-on Delay Time (Note 1)	$t_{D(ON)}$	$V_{DS}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=5.0\text{A}$, $R_G=25\Omega$ (Note 1, 2)		4		ns
Rise Time	t_R			18		ns
Turn-off Delay Time	$t_{D(OFF)}$			17		ns
Fall-Time	t_F			21		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				2	A
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=5.0\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Reverse Recovery Time (Note 1)	t_{rr}	$I_S=5.0\text{A}$, $V_{GS}=0\text{V}$		216		ns
Reverse Recovery Charge	Q_{rr}	$di/dt=100\text{A}/\mu\text{s}$ (Note1)		1477		nC

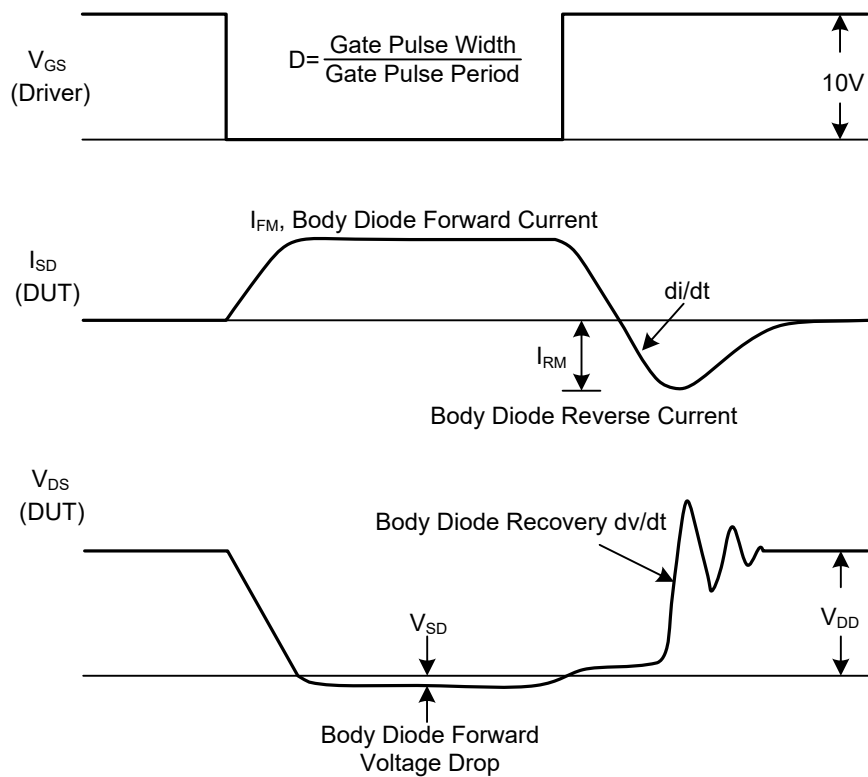
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

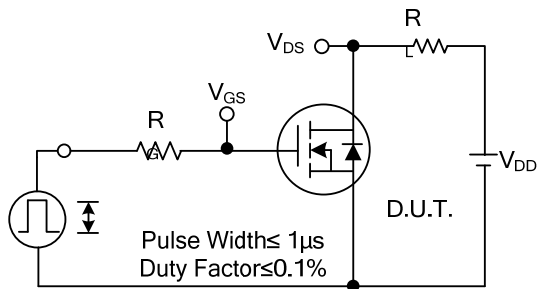


Peak Diode Recovery dv/dt Test Circuit

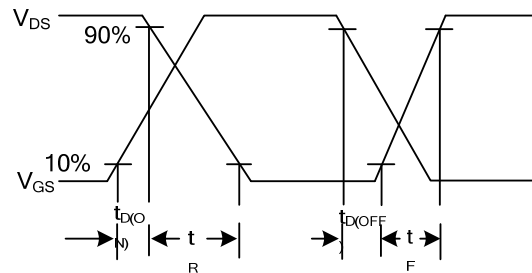


Peak Diode Recovery dv/dt Waveforms

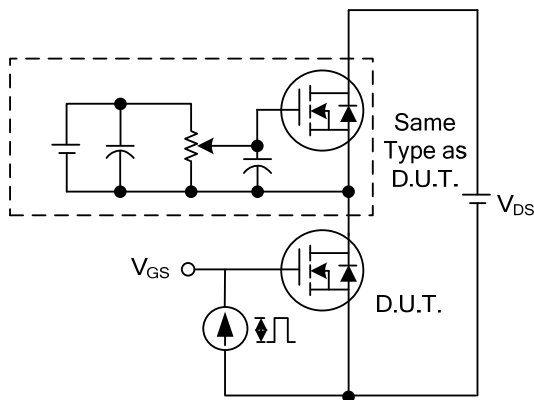
■ TEST CIRCUITS AND WAVEFORMS



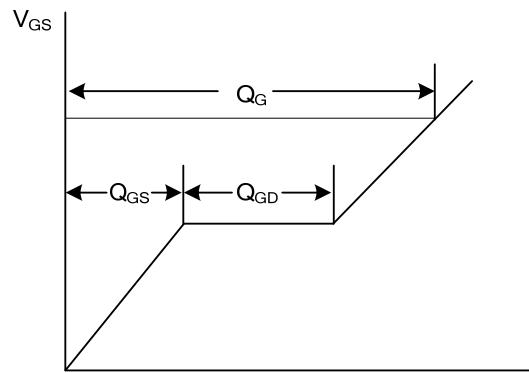
Switching Test Circuit



Switching Waveforms

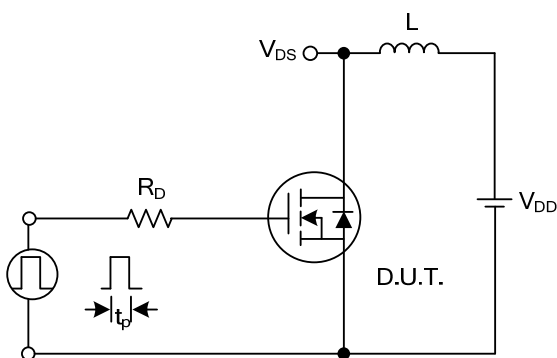


Gate Charge Test Circuit

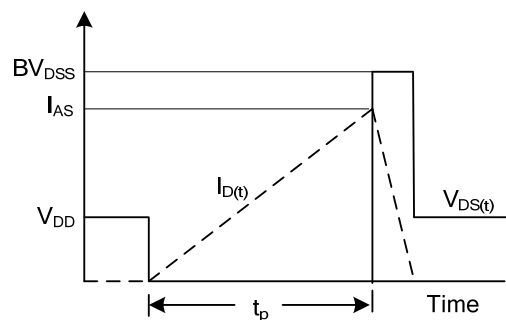


Charge

Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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