



## UT120N08H

Preliminary

Power MOSFET

### 120A, 80V N-CHANNEL POWER MOSFET

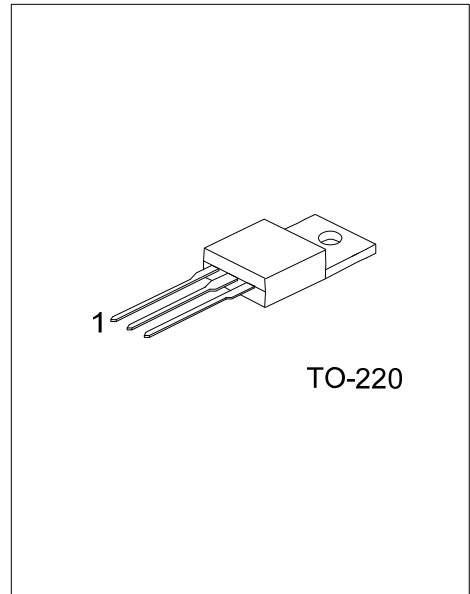
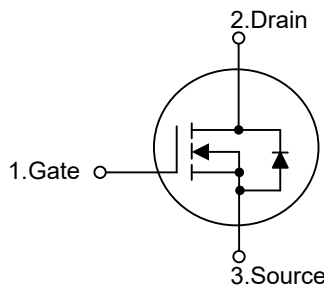
#### DESCRIPTION

The UTC **UT120N08H** is an N-channel enhancement mode Power MOSFET, it uses UTC's advanced technology to provide customers a minimum on-state resistance and high switching speed.

#### FEATURES

- \*  $R_{DS(ON)} \leq 5.0 \text{ m}\Omega @ V_{GS}=10V, I_D=60A$
- \* High switching speed
- \* Improved dv/dt capability

#### SYMBOL



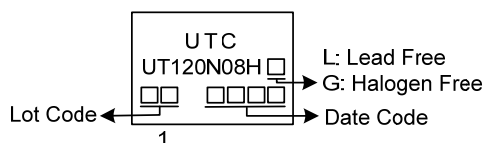
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT120N08HL-TA3-T	UT120N08HG-TA3-T	TO-220	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT120N08HG-TA3-T</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) T: Tube</p> <p>(2) TA3: TO-220</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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#### MARKING



■ ABSOLUTE MAXIMUM RATINGS (T<sub>c</sub>=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V <sub>DSS</sub>	80	V
Gate-Source Voltage		V <sub>GSS</sub>	±20	V
Drain Current	Continuous	I <sub>D</sub>	120	A
	Pulsed	I <sub>DM</sub>	240	A
Avalanche Energy	Single Pulsed	E <sub>AS</sub>	490	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.6	V/ns
Power Dissipation		P <sub>D</sub>	215	W
Junction Temperature		T <sub>J</sub>	+150	°C
Storage Temperature Range		T <sub>STG</sub>	-55 ~ +150	°C

- Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.  
 2. Repetitive Rating: Pulse width limited by maximum junction temperature.  
 3. L = 0.1mH, I<sub>AS</sub> = 99A, V<sub>DD</sub> = 30V, R<sub>G</sub> = 25Ω, Starting T<sub>J</sub> = 25°C  
 4. I<sub>SD</sub> ≤ 30A, di/dt ≤ 200A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C

■ THERMAL DATA

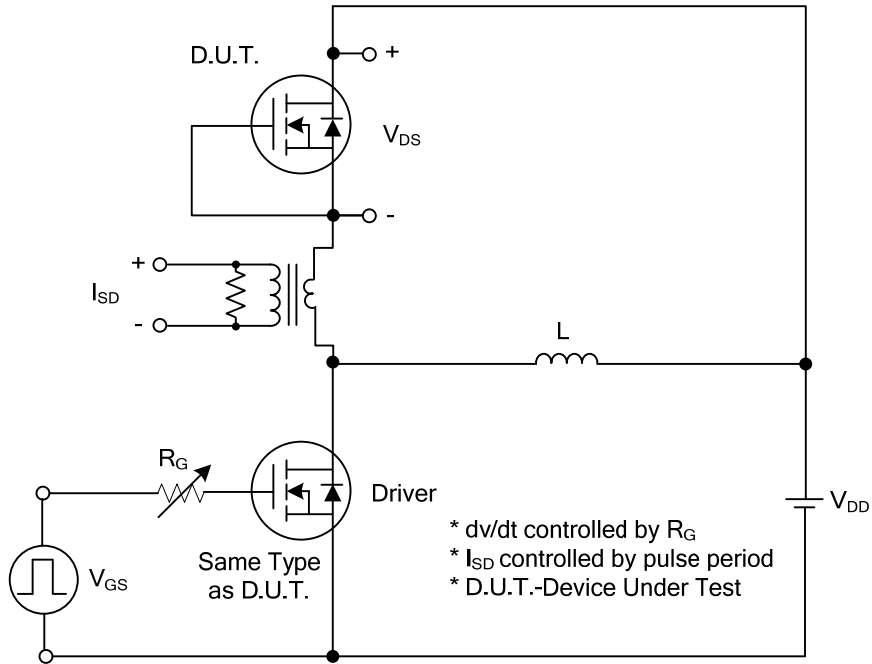
PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ <sub>JA</sub>	62.5	°C/W
Junction to Case	θ <sub>JC</sub>	0.58	°C/W

■ ELECTRICAL CHARACTERISTICS (T<sub>J</sub>=25°C, unless otherwise specified)

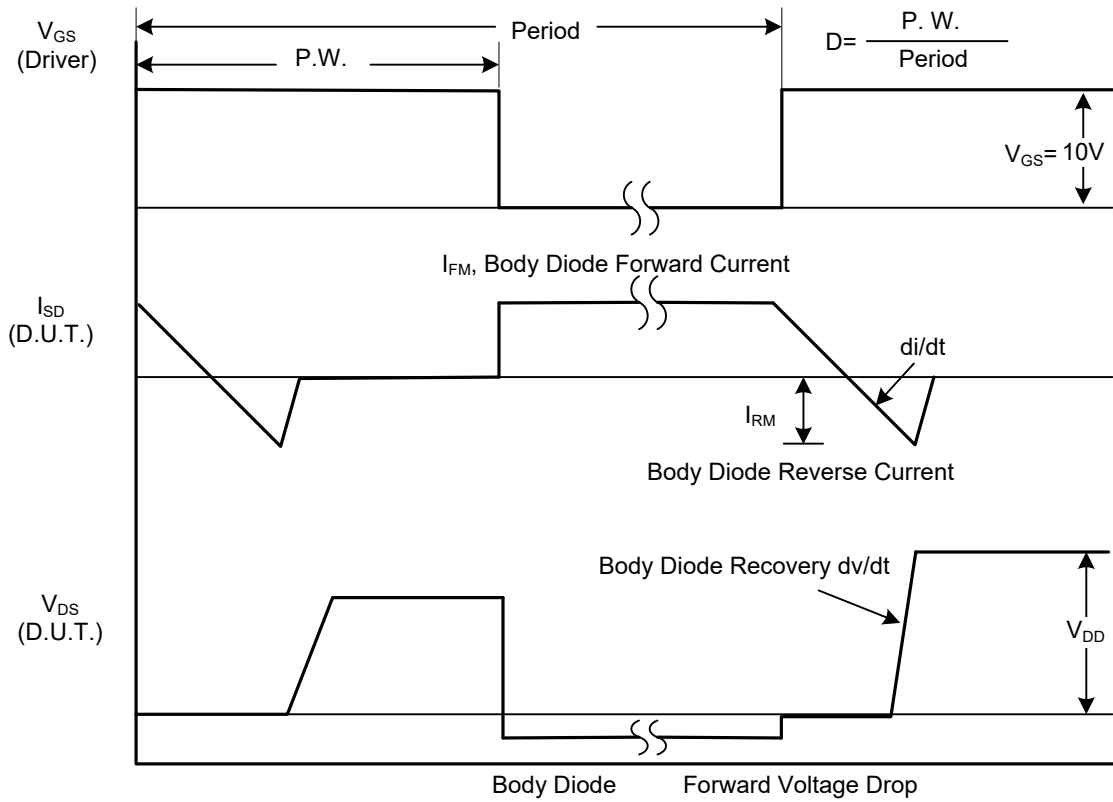
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>OFF CHARACTERISTICS</b>							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	80			V	
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V			1	μA	
Gate-Source Leakage Current	I <sub>GSS</sub>	Forward			+100	nA	
		Reverse			-100	nA	
<b>ON CHARACTERISTICS</b>							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	I <sub>D</sub> =250μA, V <sub>DS</sub> =V <sub>GS</sub>	2.0		4.0	V	
Static Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =60A			5.0	mΩ	
<b>DYNAMIC PARAMETERS</b>							
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		10.3		nF	
Output Capacitance	C <sub>OSS</sub>				828		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>				730		pF
<b>SWITCHING PARAMETERS</b>							
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> =64V, V <sub>GS</sub> =10V, I <sub>D</sub> =120A, (Note 1, 2)		284		nC	
Gate to Source Charge	Q <sub>GS</sub>			53		nC	
Gate to Drain Charge	Q <sub>GD</sub>			150		nC	
Turn-ON Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =40V, V <sub>GS</sub> =10V, I <sub>D</sub> =120A, R <sub>G</sub> =3Ω (Note 1, 2)		40		ns	
Rise Time	t <sub>r</sub>			35		ns	
Turn-OFF Delay Time	t <sub>D(OFF)</sub>			108		ns	
Fall-Time	t <sub>f</sub>			49		ns	
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>							
Maximum Body-Diode Continuous Current	I <sub>S</sub>				120	A	
Drain-Source Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =120A			1.4	V	
Reverse Recovery Time	t <sub>rr</sub>	I <sub>S</sub> =30A, V <sub>GS</sub> =0V		70		nS	
Reverse Recovery Charge (Note 1)	Q <sub>rr</sub>	dI <sub>f</sub> /dt=100A/μs		138		nC	

- Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.  
 2. Essentially independent of operating ambient temperature.

■ TEST CIRCUITS AND WAVEFORMS

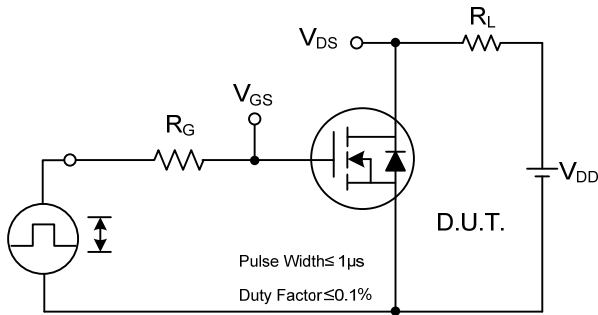


Peak Diode Recovery  $dv/dt$  Test Circuit

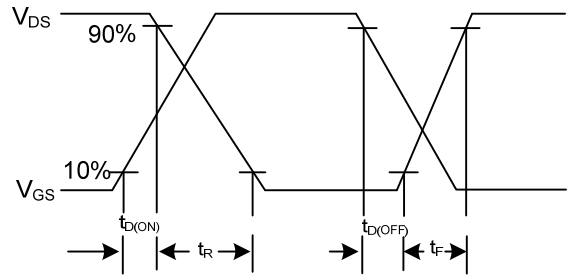


Peak Diode Recovery  $dv/dt$  Waveforms

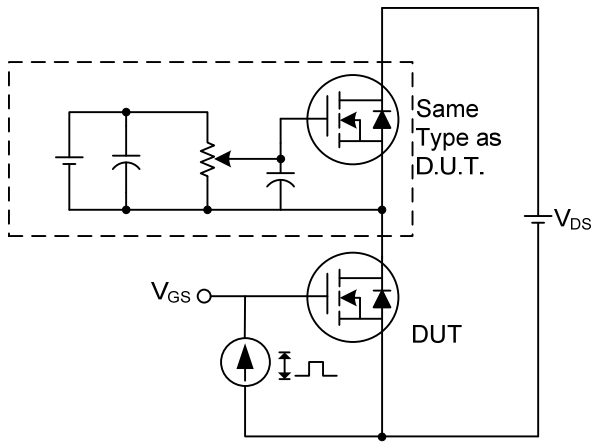
■ TEST CIRCUITS AND WAVEFORMS



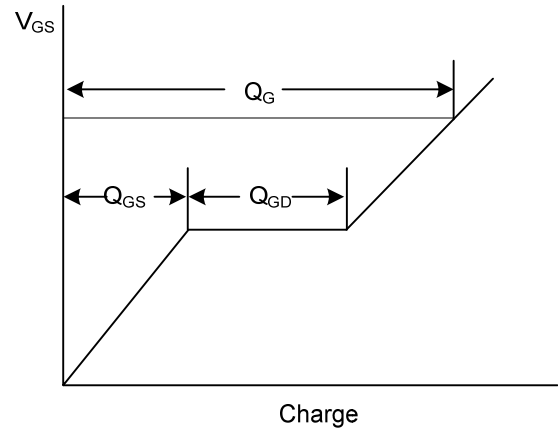
Switching Test Circuit



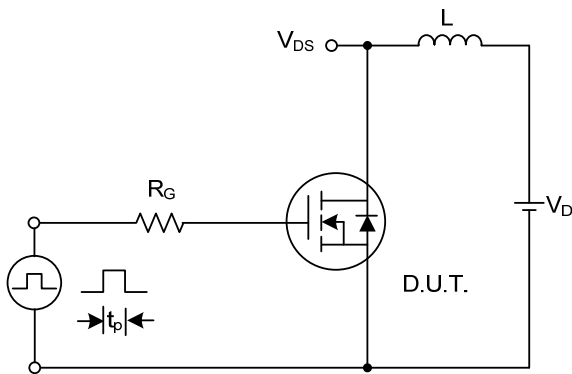
Switching Waveforms



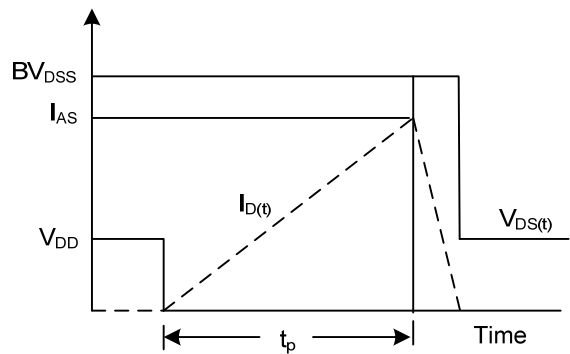
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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