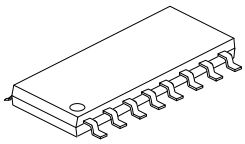
CMOS QUAD 3-STATE R/S LATCHES



SOP-16

■ DESCRIPTION

The **UCD4044B** is quad cross-coupled 3- state CMOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs.

■ FEATURES

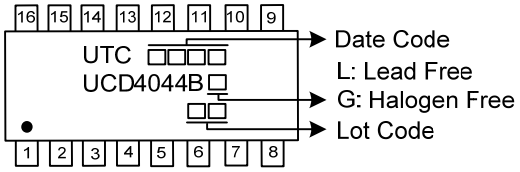
* NAND configurations
* Standardized, symmetrical output characteristics
* 100% tested for quiescent current at 20V
* Maximum input current of 100nA at 18V and 25°C
* 5V, 10V and 15V parametric ratings

■ ORDERING INFORMATION

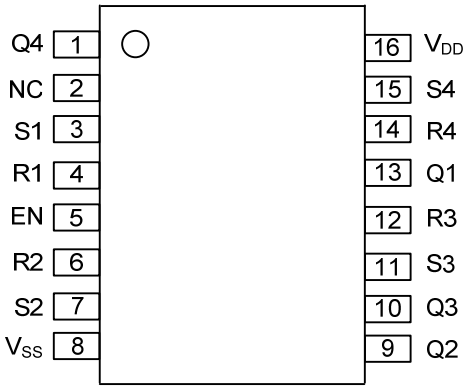
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4044BL-S16-R	UCD4044BG-S16-R	SOP-16	Tape Reel

UCD4044BG-S16-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S16: SOP-16 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

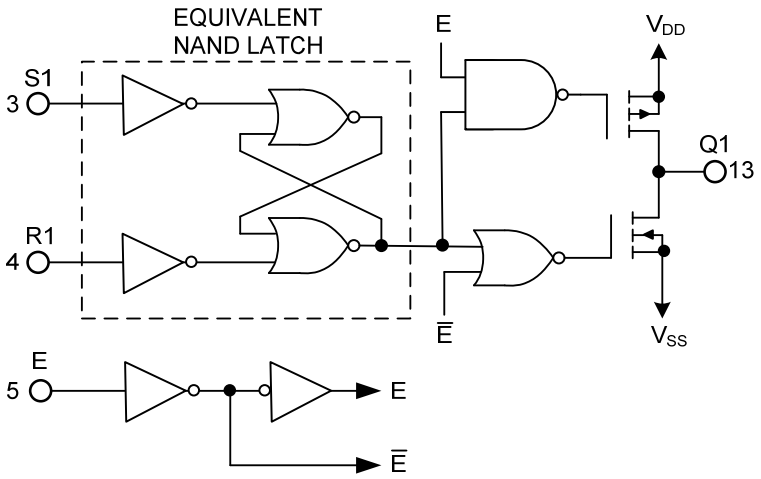


■ FUNCTION TABLE (each gate)

INPUT	INPUT	INPUT	OUTPUT
S	R	E	Q
X	X	L	OC
H	H	H	NC
L	H	H	H
H	L	H	L
L	L	H	Δ

Notes: H: HIGH Voltage Level
L: LOW Voltage Level
OC: Open Circuit
NC: No Change
Δ: Dominated by R=L Input

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
DC Supply Voltage Range (Voltages Referenced to V_{SS} Terminal)	V_{DD}		-0.5 ~ +20	V
Input Voltage Range (All Inputs)	V_{IN}		-0.5 ~ V_{DD}+0.5	V
DC Input Current, Any One Input			±10	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}	Operating	3		18	V
Input Voltage	V_{IN}		0		V_{DD}	V
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	V_{DD}=5V, V_{IN}=0,5V	4.95	5		V
		V_{DD}=10V, V_{IN}=0,10V	9.95	10		V
		V_{DD}=15V, V_{IN}=0,15V	14.95	15		V
Low-Level Output Voltage	V_{OL}	V_{DD}=5V, V_{IN}=0,5V		0	0.05	V
		V_{DD}=10V, V_{IN}=0,10V		0	0.05	V
		V_{DD}=15V, V_{IN}=0,15V		0	0.05	V
Input Low Voltage	V_{IL}	V_{DD}=5V, V_{OUT}=0.5, 4.5V			1.5	V
		V_{DD}=10V, V_{OUT}=1,9V			3	V
		V_{DD}=15V, V_{OUT}=1.5,13.5V			4	V
Input High Voltage	V_{IH}	V_{DD}=5V, V_{OUT}=0.5,4.5V	3.5			V
		V_{DD}=10V, V_{OUT}=1,9V	7			V
		V_{DD}=15V, V_{OUT}=1.5,13.5V	11			V
High-Level Output Current	I_{OH}	V_{DD}=5V, V_{IN}=0,5V, V_{OUT}=2.5V	-1.6	-3.2		mA
		V_{DD}=5V, V_{IN}=0,5V, V_{OUT}=4.6V	-0.51	-1		mA
		V_{DD}=10V, V_{IN}=0,10V, V_{OUT}=9.5V	-1.3	-2.6		mA
		V_{DD}=15V, V_{IN}=0,15V, V_{OUT}=13.5V	-3.4	-8.8		mA
Low-Level Output Current	I_{OL}	V_{DD}=5V, V_{IN}=0,5V, V_{OUT}=0.4V	0.51	1		mA
		V_{DD}=10V, V_{IN}=0,1V, V_{OUT}=0.5V	1.3	2.6		mA
		V_{DD}=15V, V_{IN}=0,15V, V_{OUT}=1.5V	3.4	8.8		mA
Input Leakage Current	$I_{I(LEAK)}$	V_{DD}=18V, V_{IN}=0,18V			±0.1	μA
3-State Output Leakage Current	I_{OUT}	V_{DD}=18V, V_{IN}=0,18V, V_{OUT}=0,18V			±0.4	μA
Quiescent Supply Current	I_{cc}	V_{DD}=5V, V_{IN}=0,5V		0.02	1	μA
		V_{DD}=10V, V_{IN}=0,10V		0.02	2	μA
		V_{DD}=15V, V_{IN}=0,15V		0.02	4	μA
		V_{DD}=20V, V_{IN}=0,20V		0.04	20	μA

■ SWITCHING CHARACTERISTICS

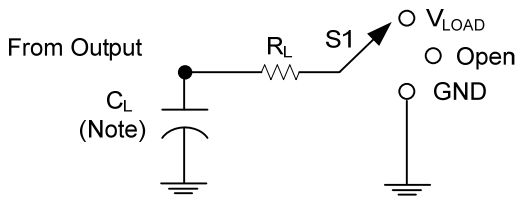
(Input: t_R=t_F=20ns, C_L=50pF, R_L=200KΩ, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay time Input(SET or RESET) to Output(Q)	t_{PHL}/t_{PLH}	V_{DD}=5V		90	300	ns
		V_{DD}=10V		42	140	ns
		V_{DD}=15V		30	100	ns
3-State Propagation Delay Time, Enable to Output(Q)	t_{PHZ}/t_{PZH}	V_{DD}=5V		55	230	ns
		V_{DD}=10V		35	110	ns
		V_{DD}=15V		23	80	ns
3-State Propagation Delay Time, Enable to Output(Q)	t_{PLZ}/t_{PZL}	V_{DD}=5V		60	180	ns
		V_{DD}=10V		35	100	ns
		V_{DD}=15V		23	70	ns
Transition Time,	t_{THL}/t_{TLH}	V_{DD}=5V		100	200	ns
		V_{DD}=10V		50	100	ns
		V_{DD}=15V		40	80	ns
Minimum SET or RESET pluse width	t_W	V_{DD}=5V		80	160	ns
		V_{DD}=10V		40	80	ns
		V_{DD}=15V		20	40	ns

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

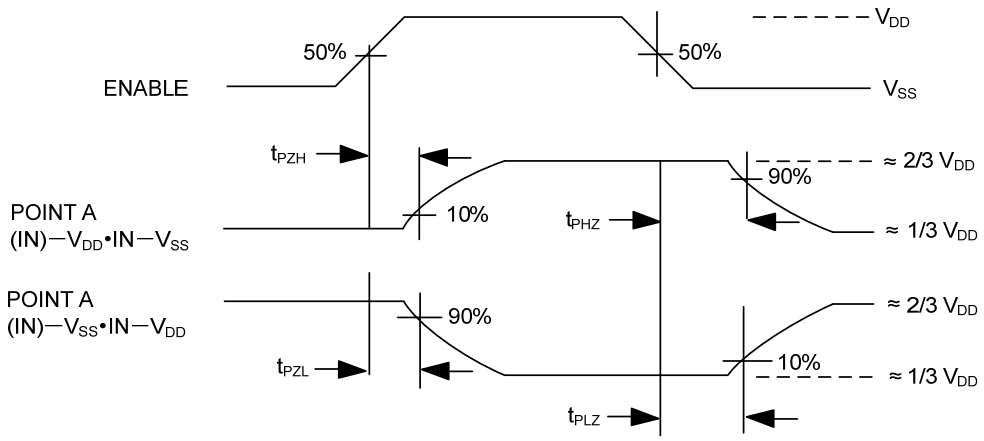
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}	Any Input		5	7.5	pF

■ TEST CIRCUIT AND WAVEFORMS



TEST	S1
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

Note: C_L includes probe and jig capacitance.



PROPAGATION DELAY TIMES

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω.

■ TEST CIRCUIT AND WAVEFORMS (Cont.)

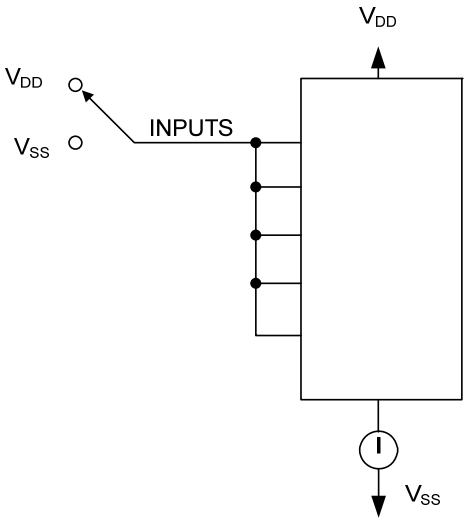


Fig. 1 Quiescent device current test circuit

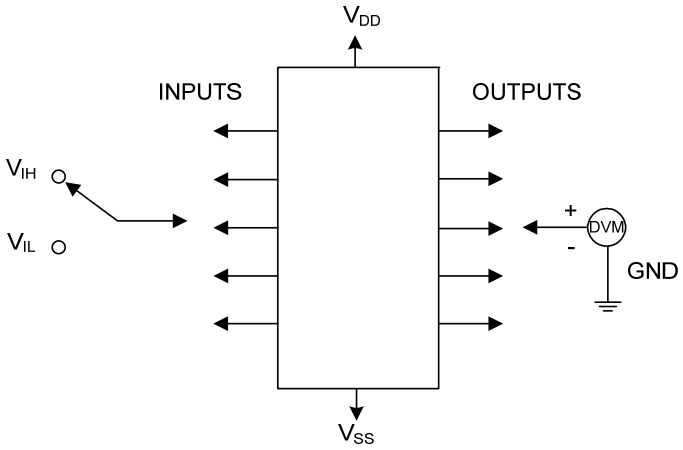


Fig. 2 Input voltage test circuit

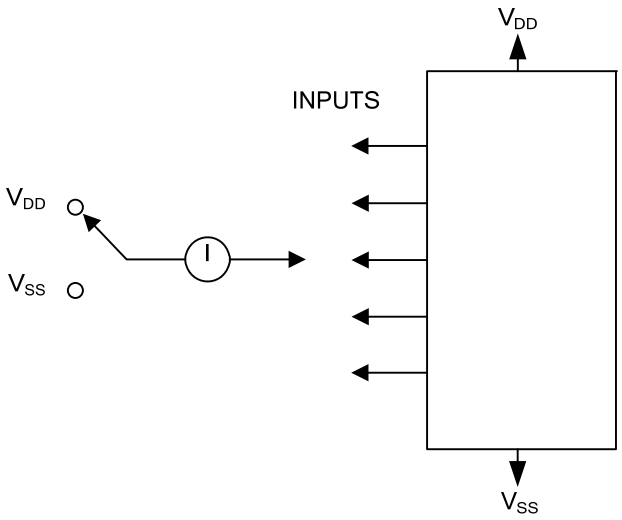


Fig. 3 Input current test circuit

Note：Measure inputs sequentially, to both V_{DD} and V_{SS}; Connect all unused inputs to either V_{DD} or V_{SS}.