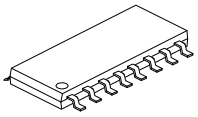
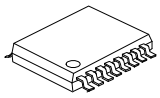
8-BIT SHIFT REGISTERS WITH LATCHED 3-STATE OUTPUT REGISTERS



SOP-16



TSSOP-16

■ DESCRIPTION

The UTC **74HCT595B** contains an 8-bit register with asynchronous reset input and an 8-bit latch with output enable input. Data on the Serial Data Input (SER) will be shift into the internal shift register during every LOW-to-HIGH transition on the Shift Clock. The latch will latch the 8-bit data from the shift register during the LOW-to-HIGH transition on the Latch Clock. The shift register also provides a serial output.

■ FEATURES

* Operation Voltage Range: 4.5V ~ 5.5V
* High Noise Immunity
* Output Compatibility with CMOS and TTL
* 8-Bit Serial-In, Parallel-Out Shift
* Inputs are TTL voltage compatiable

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT595BL-S16-R	U74HCT595BG-S16-R	SOP-16	Tape Reel
U74HCT595BL-P16-R	U74HCT595BG-P16-R	TSSOP-16	Tape Reel

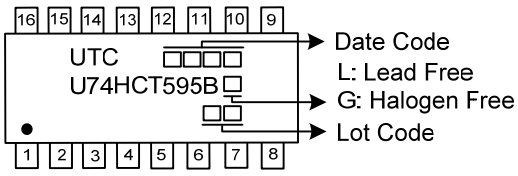
U74HCT595BG-S16-R

(1)Packing Type — (1) R: Tape Reel

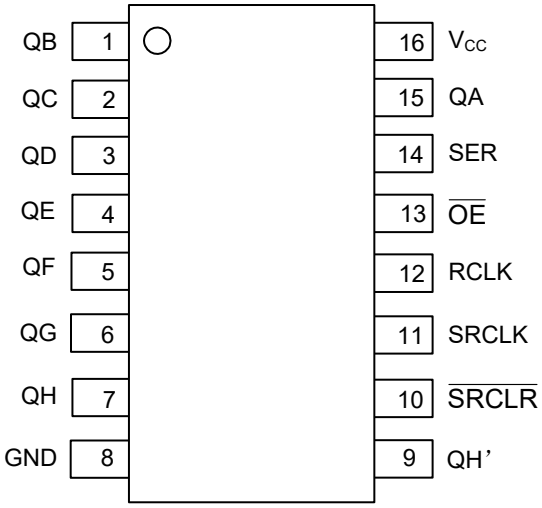
(2)Package Type — (2) S16: SOP-16, P16: TSSOP-16

(3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

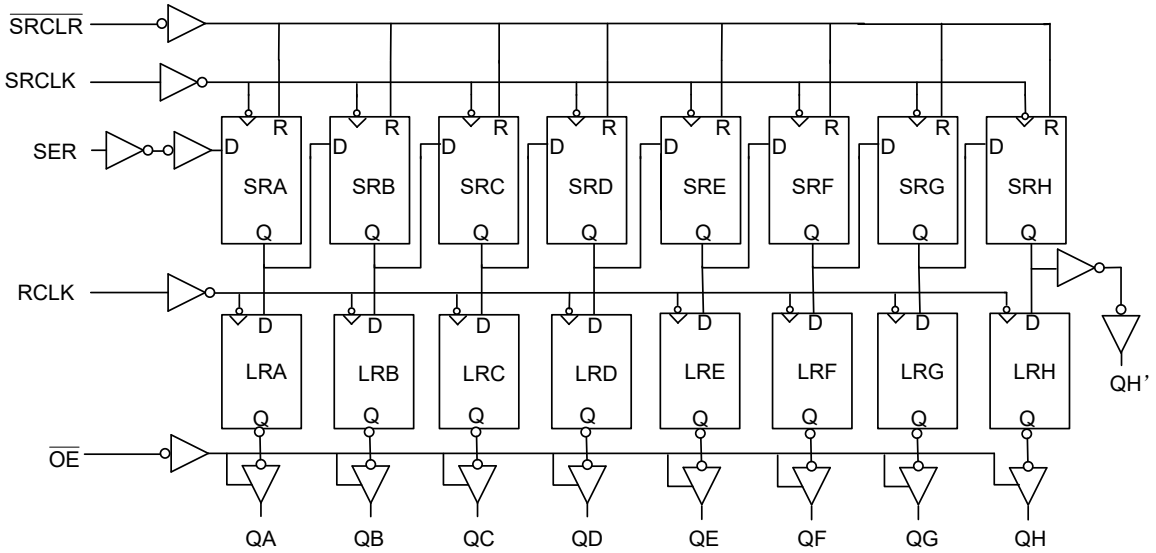


■ FUNCTION TABLE

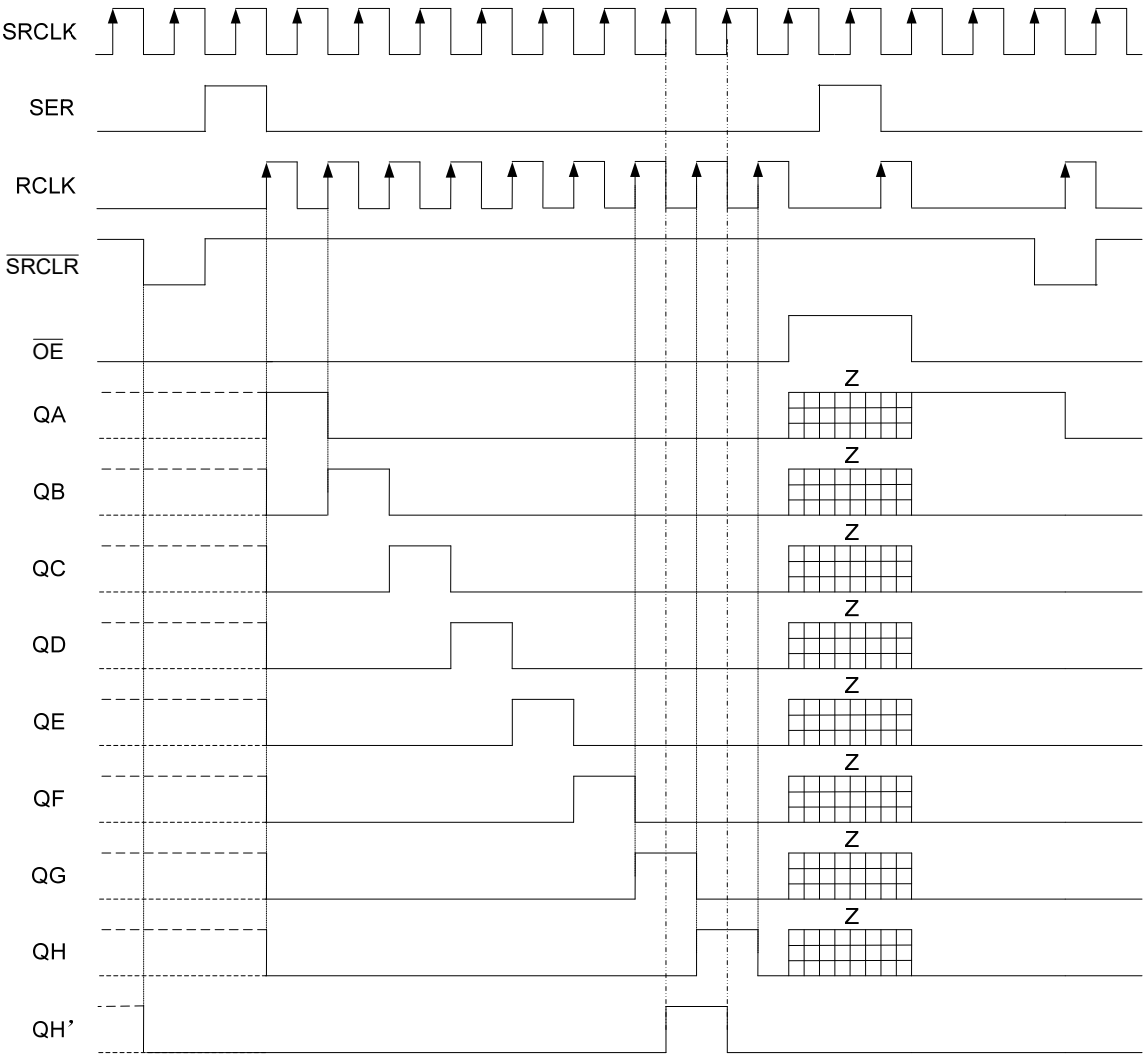
FUNCTION	INPUTS					OUTPUTS	
	SRCLK	RCLK	$\overline{OE}$	$\overline{SRCLR}$	SER	QH'	Qn
A Low-Level on $\overline{SRCLR}$ only affects the shift registers.	X	X	L	L	X	L	NC
Empty shift register loaded into storage register.	X	↑	L	L	X	L	L
Shift register clear. Parallel outputs in high-impedance OFF-state	X	X	H	L	X	L	Z
Logic high level shifted into the first shift register. Contents of all shift register stages shifted through, e.g. previous state of stage G(internal QG') appears on the serial output(QH').	↑	X	L	H	H	QG'	NC
Contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages.	X	↑	L	H	X	NC	Qn'
Contents of shift register shifted through. Previous contents of the shift register is transferred to the storage register and the parallel output stages.	↑	↑	L	H	X	QG'	Qn'

Note:H : HIGH voltage level.
L : LOW voltage level.
X : Don't care.
Z : High impedance OFF-state.
NC: No change.
↑ : Low-to-High transition.
↓ : High-to-Low transition.

■ LOGIC DIAGRAM



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
Output Voltage(active mode)	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Clamp Current (V_{IN} < 0 or V_{IN} > V_{CC})	I_{IK}	±20	mA
Output Clamp Current (V_{OUT} < 0 or V_{OUT} > V_{CC})	I_{OK}	±20	mA
Output Current (V_{OUT} = 0 or V_{CC})	I_{OUT}	±35	mA
V_{CC} or GND Current	I_{CC}	±70	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}	4.5	5	5.5	V
Input Voltage		V_{IN}	0		V_{CC}	V
Output Voltage		V_{OUT}	0		V_{CC}	V
Input Transition Rise and Fall Rate	V_{CC}=4.5V~5.5V	t_R / t_F			500	ns/V
Ambient Operating Temperature		T_A	-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	V_{CC}=4.5V~5.5V	2.0	1.6		V
Low- Level Input Voltage	V_{IL}	V_{CC}=4.5V~5.5V		1.2	0.8	V
High-Level Output Voltage, QA-QH	V_{OH}	V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.499		V
		V_{CC}=4.5V, I_{OH}=-6mA	3.98	4.3		V
Low-Level Output Voltage, QA-QH	V_{OL}	V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1	V
		V_{CC}=4.5V, I_{OL}=6mA		0.17	0.26	V
High-Level Output Voltage, QH'	V_{OH}	V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.499		V
		V_{CC}=4.5V, I_{OH}=-4mA	3.98	4.3		V
Low-Level Output Voltage, QH'	V_{OL}	V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1	V
		V_{CC}=4.5V, I_{OL}=4mA		0.15	0.26	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=5.5V, V_{IN}=V_{CC} or GND		±0.1	±100	nA
OFF-State Output Current	I_{OZ}	V_{CC}=5.5V, V_{OUT}=V_{CC} or GND		±0.01	±0.5	μA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND,I_{OUT}=0			8	μA
Additional Quiescent Supply Current	$\triangle I_{CC}$	One input at V_{CC} -2.1V,other inputs at 0 or V_{CC}		100	450	uA
Input Capacitance	C_{IN}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND		3	10	pF

■ DYNAMIC CHARACTERISTICS (T_A=25°C, C_L=50pF, R_L=1kΩ, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Clock Pulse Frequency	f_{max}	V_{CC}=4.5V	30	52		MHz
Propagation Delay From Input RCLK to Output Qn	t_{PHL}/t_{PLH}	V_{CC}=4.5V		8	40	ns
Propagation Delay From Input SRCLK to Output QH'	t_{PLH}/t_{PHL}	V_{CC}=4.5V		27	42	ns
3-state Output Enable Time From input $\overline{OE}$ to Output Qn	t_{PZH}/t_{PZL}	V_{CC}=4.5V		10	35	ns
3-state Output Enable Time From input $\overline{OE}$ to Output Qn	t_{PHZ}/t_{PLZ}	V_{CC}=4.5V		9	30	ns
Propagation Delay From Input $\overline{SRCLR}$ to Output QH'	t_{PHL}	V_{CC}=4.5V		27	40	ns
Output Transition Time, QH'	t_{TLH}/t_{THL}	V_{CC}=4.5V		8	15	ns
Output Transition Time, Qn	t_{TLH}/t_{THL}	V_{CC}=4.5V		8	12	ns

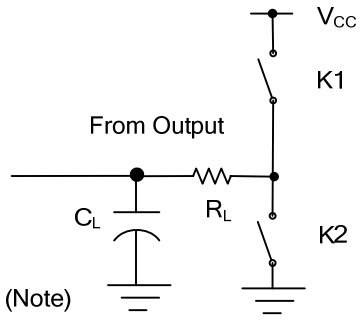
■ TIMING REQUIREMENTS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pulse Duration, SRCLK High or Low	t_W	V_{CC}=4.5V~5.5V	16	6		ns
Pulse Duration, RCLK High or Low		V_{CC}=4.5V~5.5V	16	5		ns
Pulse Duration, $\overline{SRCLR}$ Low		V_{CC}=4.5V~5.5V	20	8		ns
Setup Time, SER Before SRCLK↑	t_{SU}	V_{CC}=4.5V~5.5V	16	5		ns
Setup Time, SRCLK↑ Before RCLK↑		V_{CC}=4.5V~5.5V	16	8		ns
Hold Time, SER After SRCLK↑	t_H	V_{CC}=4.5V~5.5V	3			ns

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No Load		400		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST	K1	K2
t_{PLH}/t_{PHL}	Open	Open
t_{PHZ}/t_{PZH}	Open	Close
t_{PLZ}/t_{PZL}	Close	Open

Note: C_L includes probe and jig capacitance.