**USG10R052M** 

**Preliminary** 

**POWER MOSFET** 

PDFN5×6

# 80A, 100V N-CHANNEL SGT ENHANCEMENT POWER MOSFET

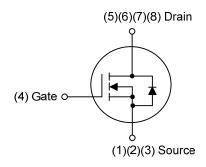
#### DESCRIPTION

The UTC  ${\sf USG10R052M}$  is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low  ${\sf R}_{\sf DS(ON)}$  characteristic by high cell density trench technology.

#### **■ FEATURES**

- \*  $R_{DS(ON)} \le 5.2 \text{ m}\Omega$  @  $V_{GS}$ =10V,  $I_D$ =30A
- \*  $R_{DS(ON)} \le 7.3 \text{ m}\Omega$  @  $V_{GS}$ =4.5V,  $I_D$ =20A
- \* Extremely low on-resistance R<sub>DS(ON)</sub>
- \* Excellent Low Ciss

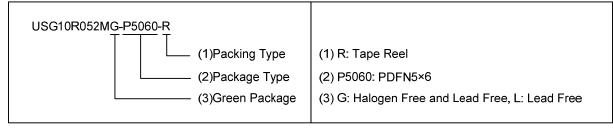




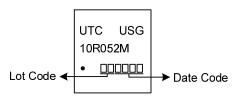
### **■ ORDERING INFORMATION**

Ordering Number		Dookogo	Pin Assignment							Dooking		
Lead Free	Halogen Free	Package	1	2	3	4	5	6	7	8	Packing	
USG10R052ML-P5060-R	USG10R052MG-P5060-R	PDFN5×6	S	S	S	G	D	D	D	D	Tape Reel	

Note: Pin Assignment: G: Gate D: Drain S: Source



#### ■ MARKING



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# ■ ABSOLUTE MAXIMUM RATING (T<sub>C</sub>=25°C unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT	
Drain-Source Voltage		$V_{DSS}$	100	V	
Gate-Source Voltage		$V_{GSS}$	±20	V	
Drain Current	DC	I <sub>D</sub>	80	Α	
	Pulsed (Note 2)	I <sub>DM</sub>	160	Α	
Avalanche Energy	Single Pulsed (Note 3)	E <sub>AS</sub>	26	mJ	
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.1	V/ns	
Power Dissipation		P <sub>D</sub>	67	W	
Junction Temperature		$T_J$	+150	°C	
Storage Temperature Range		T <sub>STG</sub>	-55 ~ <b>+</b> 150	°C	

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

- 2. Repetitive Rating: Pulse width limited by maximum junction temperature
- 3. L = 0.1mH,  $I_{AS}$  = 22.6A,  $V_{DD}$  = 50V,  $R_G$  = 25  $\Omega$ , Starting  $T_J$  = 25°C
- 4.  $I_{SD} \leq 30 A$ ,  $di/dt \leq 200 A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 25 ^{\circ} C$

#### **■ THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θЈА	65	°C/W
Junction to Case	θις	1.87	°C/W

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

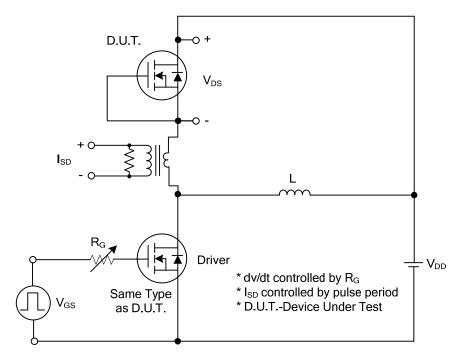
# ■ **ELECTRICAL CHARACTERISTICS** (T<sub>A</sub>=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	100			V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V			1	μΑ
Forward		V <sub>GS</sub> =+20V, V <sub>DS</sub> =0V			+100	nA
Gate-Source Leakage Current Reverse	I <sub>GSS</sub>	V <sub>GS</sub> =-20V, V <sub>DS</sub> =0V			-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	1.0		2.5	V
Static Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	$V_{GS}$ =10V, $I_D$ =30A			5.2	mΩ
Static Drain-Source On-State Resistance		$V_{GS}$ =4.5V, $I_D$ =20A			7.3	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C <sub>ISS</sub>			3551		pF
Output Capacitance	Coss	$V_{GS}$ =0V, $V_{DS}$ =25V, f=1.0MHz		1821		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			240		pF
SWITCHING PARAMETERS						
Total Gate Charge	$Q_G$	-\/ -90\/ \/ -10\/   -90A		90		nC
Gate to Source Charge	Q <sub>G</sub> s	V <sub>DS</sub> =80V, V <sub>GS</sub> =10V, I <sub>D</sub> =80A (Note 1, 2)		10		nC
Gate to Drain Charge	$Q_GD$	(Note 1, 2)		37		nC
Turn-ON Delay Time	t <sub>D(ON)</sub>			13		ns
Rise Time	t <sub>R</sub>	V <sub>DD</sub> =50V, V <sub>GS</sub> =10V, I <sub>D</sub> =80A,		22		ns
Turn-OFF Delay Time	t <sub>D(OFF)</sub>	R <sub>G</sub> =3Ω (Note 1, 2)		53		ns
Fall-Time	t <sub>F</sub>			27		ns
SOURCE-DRAIN DIODE RATINGS AND	CHARACTER	ISTICS				
Maximum Continuous Drain-Source Diode	Is				80	Α
Forward Current					80	А
Maximum Pulsed Drain-Source Diode	Ism				160	Α
Forward Current	ISM				100	^
Diode Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> =80A, V <sub>GS</sub> =0V			1.4	V
Reverse Recovery Time (Note 1)	t <sub>rr</sub>	Is=30A, V <sub>GS</sub> =0V,		63		nS
Reverse Recovery Charge	Qrr	dI <sub>F</sub> /dt =100A/μs		131		nC

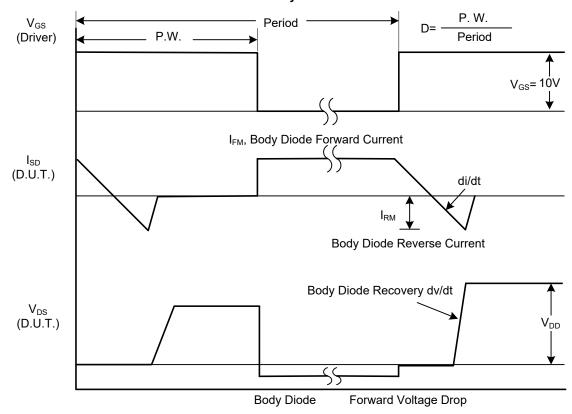
Notes: 1. Pulse Test: Pulse width ≤ 300µs, Duty cycle ≤ 2%.

<sup>2.</sup> Essentially independent of operating temperature.

# ■ TEST CIRCUITS AND WAVEFORMS

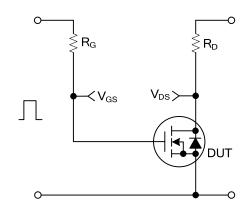


# Peak Diode Recovery dv/dt Test Circuit



Peak Diode Recovery dv/dt Waveforms

# **■ TEST CIRCUITS AND WAVEFORMS**



90%

10%

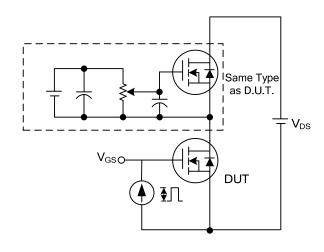
t<sub>d(ON)</sub> t<sub>R</sub>

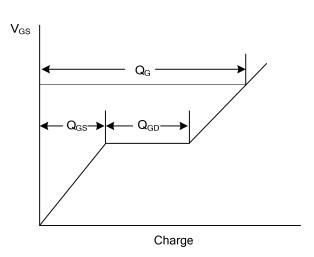
t<sub>ON</sub>

t<sub>OFF</sub>

itching Test Circuit

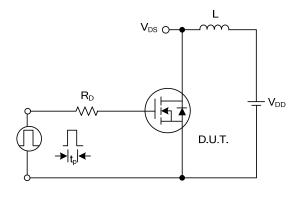
**Switching Waveforms** 

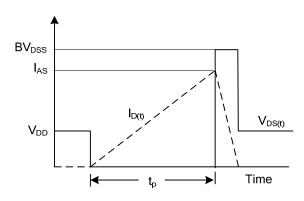




**Gate Charge Test Circuit** 

**Gate Charge Waveform** 





**Unclamped Inductive Switching Test Circuit** 

**Unclamped Inductive Switching Waveforms** 

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