



45NM65S-U3

Preliminary

Power MOSFET

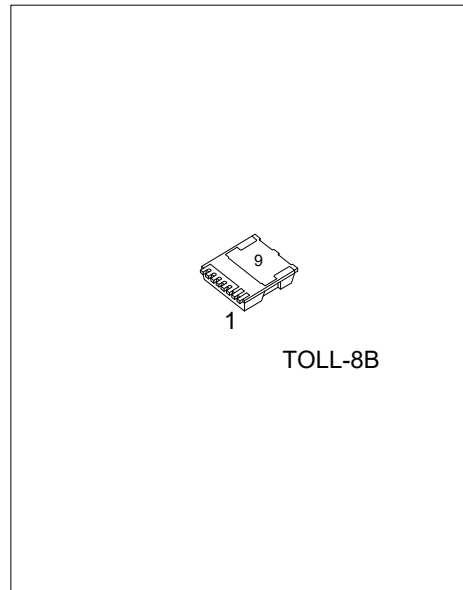
45A, 650V N-CHANNEL SUPER-JUNCTION MOSFET

DESCRIPTION

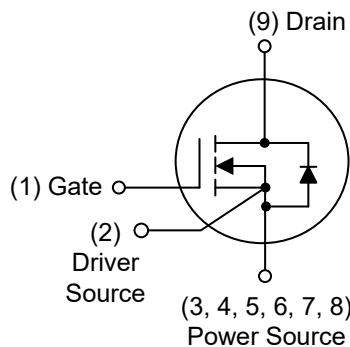
The **UTC 45NM65S-U3** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at AC-DC converters for power applications.

FEATURES

- * $R_{DS(ON)} \leq 0.89 \Omega$ @ $V_{GS}=10V, I_D=22.5A$
- * Fast switching capability
- * Avalanche energy tested
- * Improved dv/dt capability, high ruggedness



SYMBOL



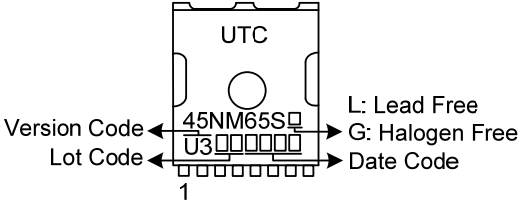
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment					Packing
Lead Free	Halogen Free		1	2	3	4	5	
45NM65SL-U3-K04-8080-R	45NM65SG-U3-K04-8080-R	DFN8080-4	G	S	S	S	D	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

45NM65SG-U3-K04-8080-R	(1)Packing Type	(1) R: Tape Reel
	(2)Package Type	(2) K04-8080: DFN8080-4
	(3)Version Code	(3) Version U3
	(4)Green Package	(4) G: Halogen Free and Lead Free, L: Lead Free

MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	650	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	45	A
	Pulsed (Note 2)			A
Avalanche Energy		E_{AS}	3600	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	3.4	V/ns
Power Dissipation		P_D	240	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 100\text{mH}$, $I_{AS} = 8.5\text{A}$, $V_{DD} = 90\text{V}$, $R_G = 25\Omega$ Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	35	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	0.46 (Note)	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate P_c board, 2oz copper, with 1inch square copper plate.

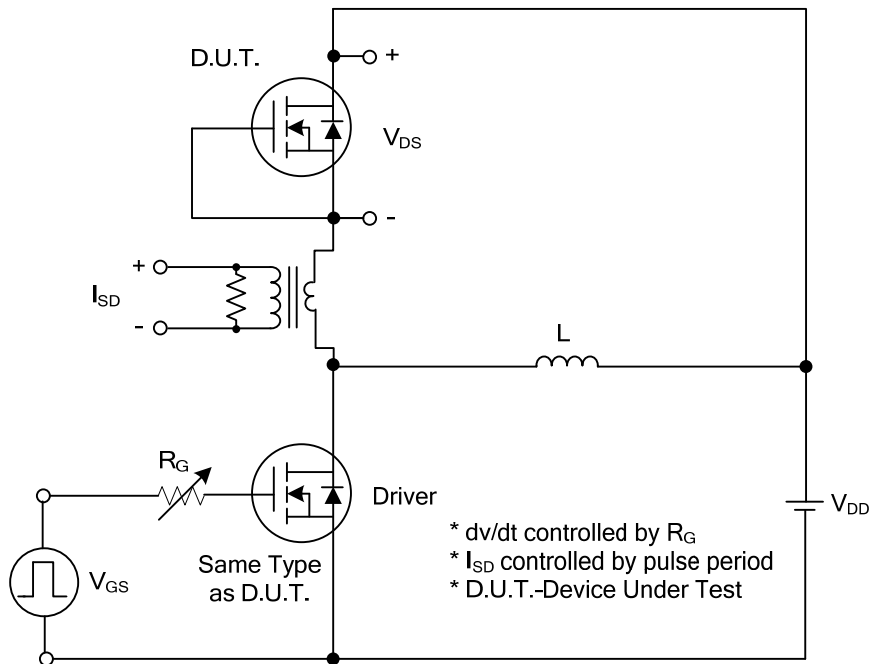
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	650			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =650V, V _{GS} =0V			100	nA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	2.5		4.5	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =22.5A			89	mΩ
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =50V, f=1MHz		4511		pF
Output Capacitance	C _{OSS}			649		pF
Reverse Transfer Capacitance	C _{RSS}			0.2		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge (Note 1)	Q _G	V _{DS} =520V, V _{GS} =10V, I _D =45A (Note 1, 2)		112		nC
Gate-Source Charge	Q _{GS}			30		nC
Gate-Drain Charge	Q _{DD}			44		nC
Turn-On Delay Time (Note 1)	t _{D(ON)}	V _{DD} =100V, V _{GS} =10V, I _D =45A, R _G =25Ω (Note 1, 2)		64		ns
Turn-On Rise Time	t _R			38		ns
Turn-Off Delay Time	t _{D(OFF)}			268		ns
Turn-Off Fall Time	t _F			77		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I _S				45	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				135	A
Drain-Source Diode Forward Voltage (Note 1)	V _{SD}	I _S =45A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t _{rr}	I _S =30A, V _{GS} =0V, dI _F /dt=100A/μs		540		nS
Body Diode Reverse Recovery Charge	Q _{rr}			9984		nC

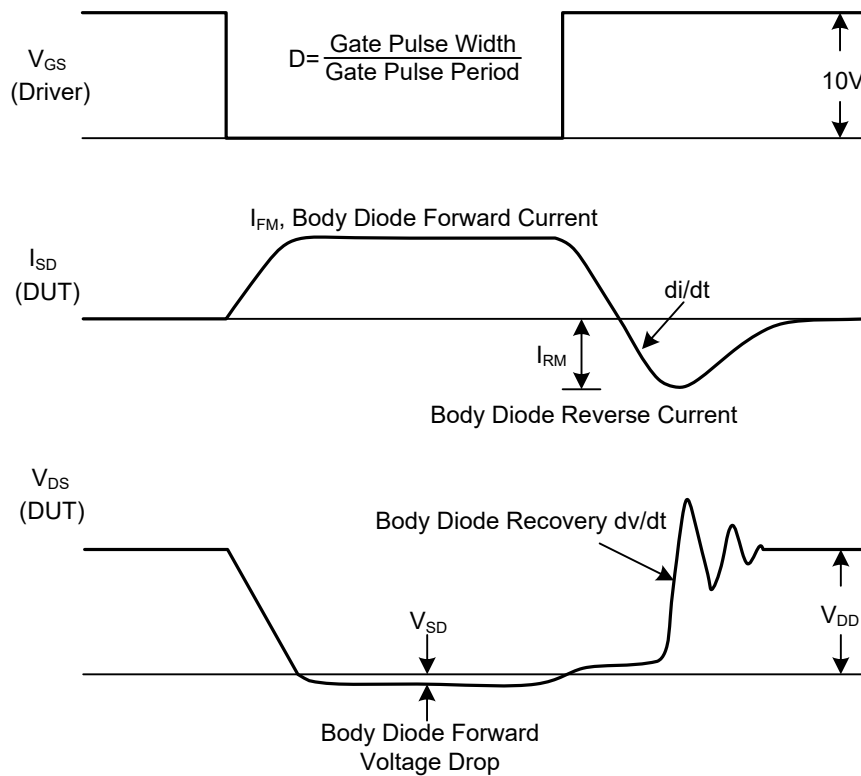
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

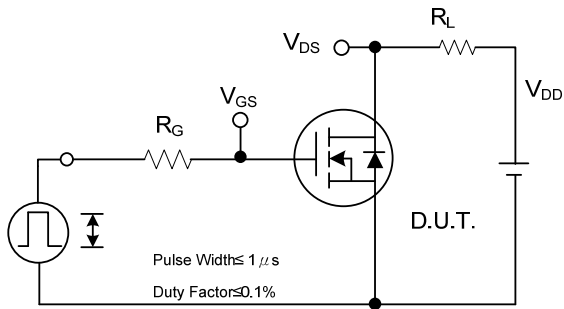


Peak Diode Recovery dv/dt Test Circuit

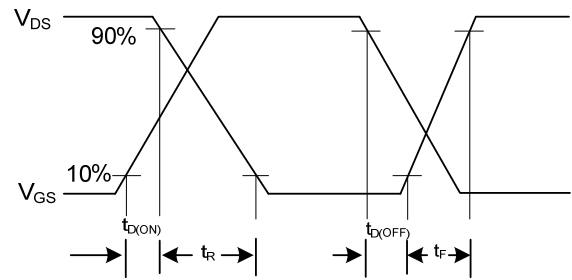


Peak Diode Recovery dv/dt Waveforms

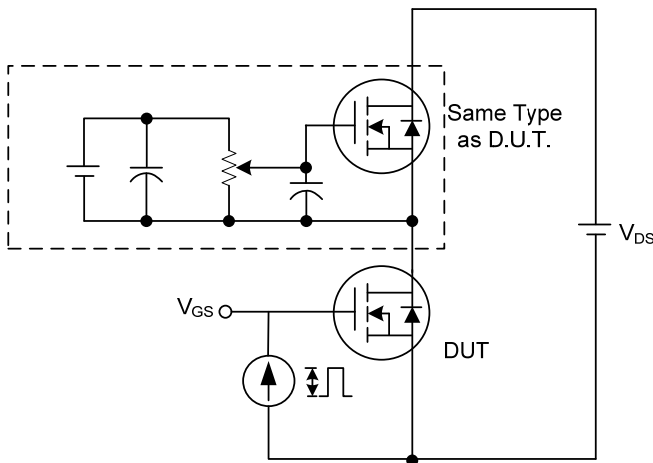
■ TEST CIRCUITS AND WAVEFORMS



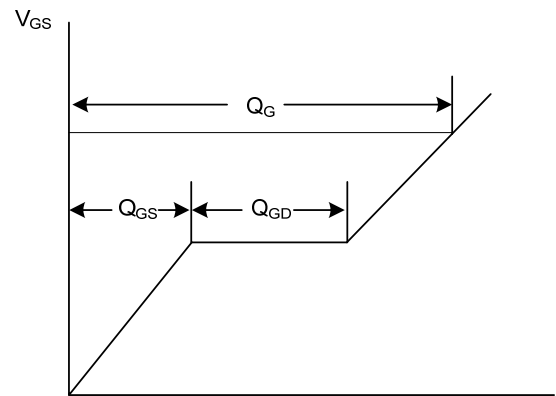
Switching Test Circuit



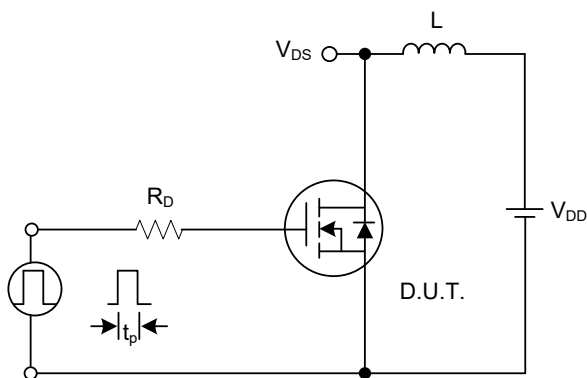
Switching Waveforms



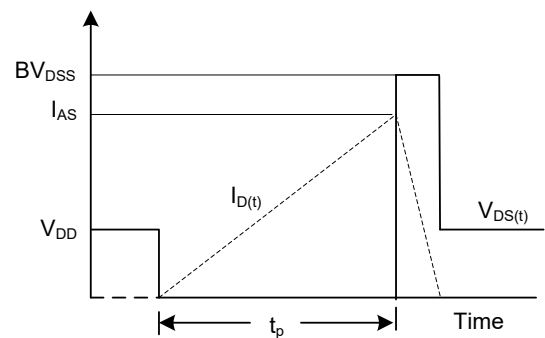
Gate Charge Test Circuit



Charge
Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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