UPGE80N33W

**Preliminary** 

Insulated Gate Bipolar Transistor

# 330V, SMPS N-CHANNEL IGBT

#### ■ DESCRIPTION

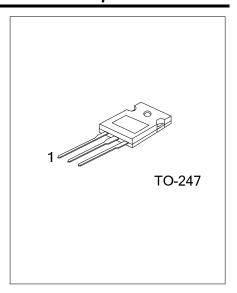
The UTC **UPGE80N33W** is a N-channel IGBT. it uses UTC's advanced technology to provide customers with high input impedance, high switching speed and low conduction loss, etc.

The UTC **UPGE80N33W** is suitable for high voltage switching, high frequency switch mode power supplies.

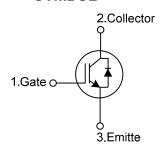
#### ■ FEATURES

- \* High switching speed
- \* High avalanche ruggedness
- \* Low saturation voltage:

V<sub>CE(SAT).Typ.</sub> = 2.09V @ I<sub>C</sub>=80A, V<sub>GE</sub>=15V (T<sub>C</sub> =25°C)



### ■ SYMBOL



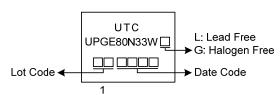
### ■ ORDERING INFORMATION

Ordering Number		Daalaaaa	Pin Assignment			Dli	
Lead Free	Halogen Free	Package	1	2	3	Packing	
UPGE80N33WL-T47-T	UPGE80N33WG-T47-T	TO-247	G	С	Е	Tube	

Note: Pin Assignment: G: Gate C: Collector E: Emitter

UPGE80N33WG-T47-T
(1)Packing Type (1) T: Tube
(2)Package Type (2) T47: TO-247
(3)Green Package (3) G: Halogen Free and Lead Free, L: Lead Free

### **■ MARKING**



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## ■ **ABSOLUTE MAXIMUM RATINGS** (T<sub>C</sub>=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Collector-Emitter Voltage		V <sub>CES</sub>	330	V
Gate-Emitter Voltage		\ /	±20	V
Transient Gate-emitter voltage (tp < 5 ms)		$V_{GES}$	±25	V
Continuous Collector Current	T <sub>C</sub> =25°C	Ic	160	Α
	T <sub>C</sub> =100°C		80	Α
Collector Current Pulsed (Note 1)		I <sub>CM</sub>	220	Α
Diode Forward Current	T <sub>C</sub> =25°C	I <sub>F</sub>	80	Α
	T <sub>C</sub> =100°C		40	Α
Short Circuit Withstand Time $V_{GE} = 15V, V_{CC} \le 200V$		tsc		
				μs
Allowed number of short circuits < 1000			10	
Time between short circuits: ≥ 1.0s				
$T_{VJ} = 25^{\circ}\text{C}$				
Power Dissipation (T <sub>C</sub> =25°C)		P <sub>D</sub>	270	W
Operating Junction Temperature		$T_J$	-40 ~ +150	°C
Storage Temperature Range		T <sub>STG</sub>	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are stress ratings only and functional device operation is not implied. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

## **■ THERMAL DATA**

PARAMETER	SYMBOL	RATING	UNIT
Junction to Case	θјς	0.46	°C/W

<sup>2.</sup> Pulse width limited by maximum junction temperature.

# ■ **ELECTRICAL CHARACTERISTICS** (T<sub>C</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT	
Off Characteristics								
Collector-Emitter Breakdown Voltage	BV <sub>CES</sub>			330			V	
Collector Cut-Off Current	I <sub>CES</sub>	V <sub>CE</sub> =330V, V <sub>GE</sub> =0V				5	μΑ	
G-E Leakage Current	I <sub>GES</sub>	V <sub>CE</sub> =0V, V <sub>GE</sub> =±20V				±400	nA	
On Characteristics								
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	I <sub>C</sub> =250μA, V <sub>CE</sub> =V <sub>GE</sub>		4.5		7.5	V	
Collector to Emitter Saturation Voltage	V <sub>CE(SAT)</sub>	I <sub>C</sub> =80A, V <sub>GE</sub> =15V	T <sub>C</sub> =25°C		2.09	2.3	V	
			T <sub>C</sub> =125°C		2.49		V	
Dynamic Characteristics				ā.	ā.			
Input Capacitance	CIES			4110		рF		
Output Capacitance	Coes	V <sub>CE</sub> =25V, V <sub>GE</sub> =0V, f=1MHz			355		рF	
Reverse Transfer Capacitance	C <sub>RES</sub>				49		pF	
Switching Characteristics								
Total Gate Charge	$Q_{G}$				92		nC	
Gate-Emitter Charge	$Q_GE$	V <sub>CE</sub> =280V, I <sub>C</sub> =80A, V <sub>GE</sub> =15V			28		nC	
Gate-Collector Charge	$Q_GC$				1.8		nC	
Turn-On Delay Time	t <sub>DON)</sub>				27		ns	
Rise Time	$t_R$				57		ns	
Turn-Off Delay Time	t <sub>DOFF)</sub>	V <sub>CC</sub> =240V, I <sub>C</sub> =80A, R <sub>G</sub> =5Ω, V <sub>GE</sub> =0~15V, L=500μH			120		ns	
Fall Time	$t_{F}$				474		ns	
Turn-On Switching Loss	Eon				1.77		mJ	
Turn-Off Switching Loss	E <sub>OFF</sub>	]			3.78		mJ	
SOURCE- DRAIN DIODE RATINGS A	ND CHARAC	TERISTICS						
Forward Voltage Drop	$V_{F}$	I <sub>F</sub> =40A				2.0	V	
Reverse Recovery Time	t <sub>rr</sub>	-I <sub>F</sub> =80A, dI/dt=100A/μS, V <sub>CC</sub> =240V			28		ns	
Reverse Recovery Charge	$Q_{rr}$				233		nC	

### ■ TEST CIRCUIT AND WAVEFORMS

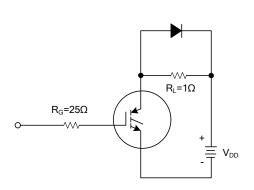


Fig 1. INDUCTIVE SWITCHING TEST CIRCUIT

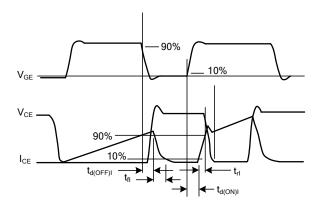


Fig 2. SWITCHING TEST WAVEFORMS

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