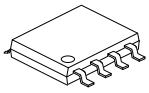
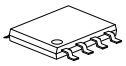
ULSF0102

CMOS IC

2 CHANNEL AUTO-BIDIRECTIONAL MULTI-VOLTAGE LEVEL TRANSLATOR FOR OPEN-DRAIN APPLICATION



SOP-8



MSOP-8

CDFN2030-8

X2DFN1410-8

■ DESCRIPTION

The UTC **ULSF0102** family supports up to 100MHz up translation and greater than 100MHz down translation at≤30pF cap load and up to 40MHz up/down translation at 50pF cap load which allows the UTC **ULSF0102** family to support more consumer or telecom interfaces (MDIO or SDIO). The UTC **ULSF0102** family has bidirectional voltage translation without the need for DIR pin which minimizes system effort (for PM Bus, I^2C, or SM Bus).

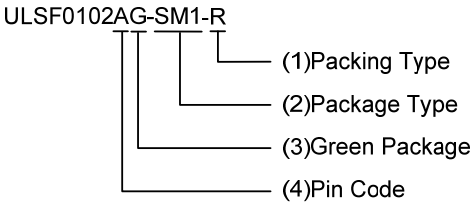
The UTC **ULSF0102** family supports 5V tolerance on I/O port which makes it compatible with TTL levels in industrial and telecom applications. The UTC **ULSF0102** family is able to setup different voltage translation levels on each channel which makes it very flexible.

■ FEATURES

* Provides bidirectional voltage translation with no direction pin
* Supports up to 100MHz up translation and greater than 100MHz down translation at ≤ 30pF cap load and up to 40MHz up/down translation at 50pF cap load.
* Allow bidirectional voltage level translation between
  – 0.95V↔1.8/2.5/3.3/5V
  – 1.2V↔1.8/2.5/3.3/5V
  – 1.8V↔2.5/3.3/5V
  – 2.5V↔3.3/5V
  – 3.3V↔5V
* Low standby current
* 5V tolerance I/O port to support TTL
* Low R_{ON} provides less signal distortion
* High-Impedance I/O pins for EN=Low

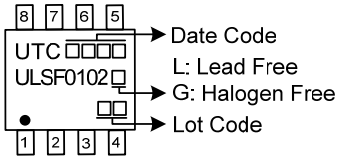
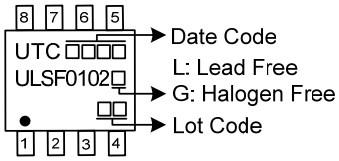
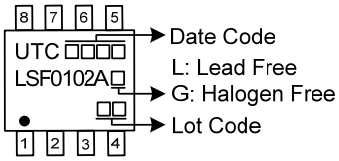
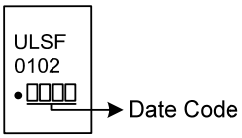
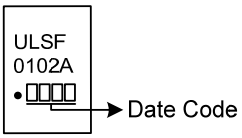
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
ULSF0102L-S08-R	ULSF0102G-S08-R	SOP-8	Tape Reel
ULSF0102L-SM1-R	ULSF0102G-SM1-R	MSOP-8	Tape Reel
ULSF0102L-CK08-2030-R	ULSF0102G-CK08-2030-R	CDFN2030-8	Tape Reel
ULSF0102AL-SM1-R	ULSF0102AG-SM1-R	MSOP-8	Tape Reel
ULSF0102AL-CK08-2030-R	ULSF0102AG-CK08-2030-R	CDFN2030-8	Tape Reel
ULSF0102AL-KAD-R	ULSF0102AG-KAD-R	X2DFN1410-8	Tape Reel

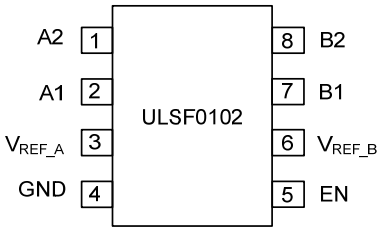


(1) R: Tape Reel
(2) S08: SOP-8, SM1: MSOP-8
CK08-2030: CDFN2030-8, KAD: X2DFN1410-8
(3) G: Halogen Free and Lead Free, L: Lead Free
(4) Refer to PIN CONFIGURATION

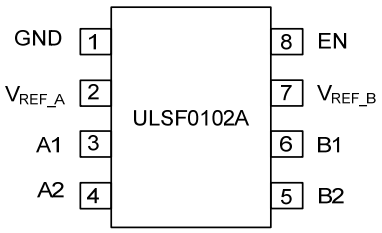
■ MARKING

PACKAGE	ULSF0102	ULSF0102A
SOP-8		-
MSOP-8		
CDFN2030-8		
X2DFN1410-8	-	

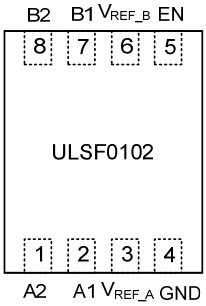
■ PIN CONFIGURATION



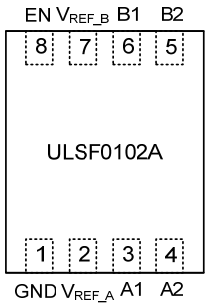
SOP-8 / MSOP-8



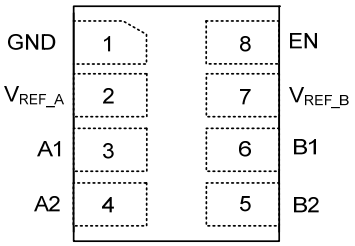
MSOP-8



CDFN2030-8
(Top View)



CDFN2030-8
(Top View)

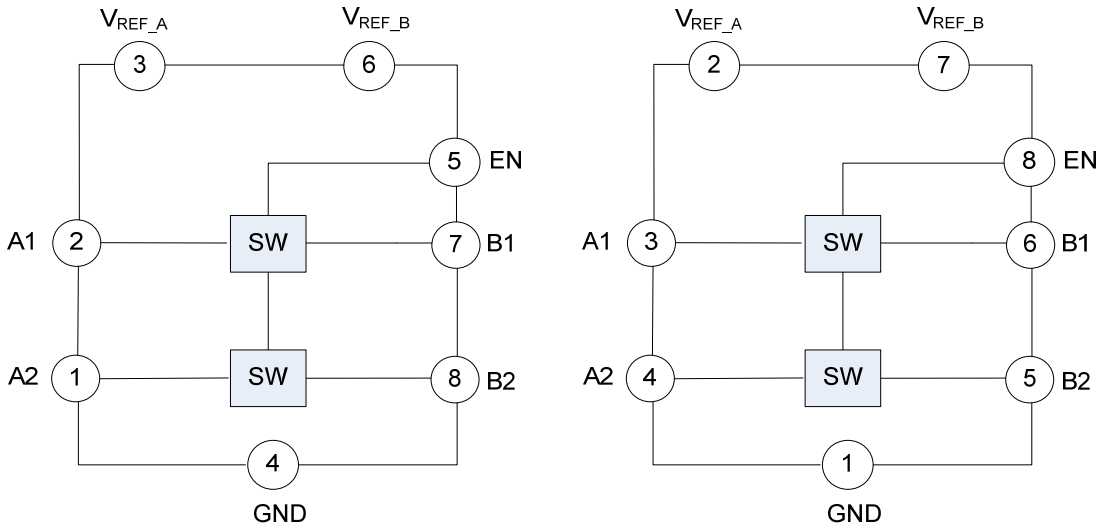


ULSF0102A
X2DFN1410-8
(TOP VIEW)

■ PIN DESCRIPTION

PIN NO.		PIN NAME	DESCRIPTION
ULSF0102	ULSF0102A		
4	1	GND	Ground
3	2	V_{REF_A}	Reference supply voltage
1, 2	3, 4	An	Data port
7 ,8	5, 6	Bn	Data port
6	7	V_{REF_B}	Reference supply voltage
5	8	EN	Switch enable input; connect to V_{REF_B} and pull-up through a high R(200K)

■ BLOCK DIAGRAM



■ FUNCTION TABLE

INPUT EN PIN	FUNCTION
H	An = Bn
L	H-Z

Note: EN is controlled by V_{REF_B} logic levels.

■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Input Voltage (Note 3)	V_{IN}		-0.5 ~ 7	V
Input/output Voltage (Note 3)	$V_{I/o}$		-0.5 ~ 7	V
Continuous channel current			128	mA
Input Clamp Current	I_{IK}	V_{IN}<0V	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input/output Voltage	$V_{I/O}$		0		5.5	V
Reference Voltage	$V_{REF\_A/B/EN}$		0		5.5	V
Pass transistor current	I_{PASS}				64	mA
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C , unless otherwise specified)

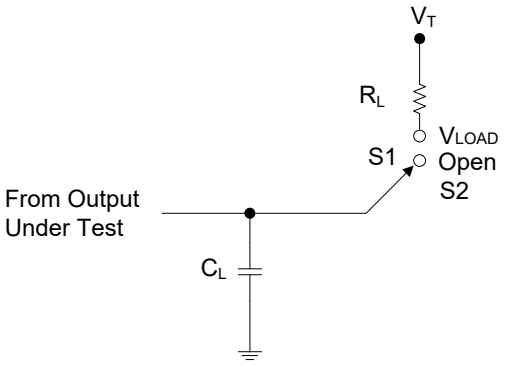
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input clamp Voltage	V_{IK}	I_I=-18mA ,V_{EN}=0				-1.2	V
Input Leakage Current	I_{IH}	V_{IN}=5V , V_{EN}=0				5	μA
Quiescent Supply Current	I_{CC}	V_{REF_B}=V_{EN}=5.5V, V_{REF_A}=4.5V or 1V, I_O=0, V_I=V_{CC} or GND			6		μA
Input Capacitance	C_{IN}	V_I=3V or 0			11		pF
Off Capacitance	$C_{IO(OFF)}$	V_I=3V or 0, V_{EN}=0			7		pF
Capacitance When Switch Is Enabled	$C_{IO(ON)}$	V_I=3V or 0, V_{EN}=3V			16.5		pF
Switch On Resistance (Note 2)	R_{ON}	V_I=0, I_O=64mA	V_{REF_A}=3.3V, V_{REF_B}=V_{EN}=5V		7		Ω
			V_{REF_A}=1.8V, V_{REF_B}=V_{EN}=5V		8		Ω
			V_{REF_A}=1.0V, V_{REF_B}=V_{EN}=5V		9		Ω
		V_I=0, I_O=32mA	V_{REF_A}=1.8V, V_{REF_B}=V_{EN}=5V		10		Ω
			V_{REF_A}=2.5V, V_{REF_B}=V_{EN}=5V		11		Ω
		V_I=1.8V, I_O=15mA	V_{REF_A}=3.3V, V_{REF_B}=V_{EN}=5V		8		Ω
		V_I=1V, I_O=10mA	V_{REF_A}=1.8V, V_{REF_B}=V_{EN}=3.3V		12		Ω
		V_I=0, I_O=10mA	V_{REF_A}=1.0V, V_{REF_B}=V_{EN}=3.3V		14		Ω
		V_I=0, I_O=10mA	V_{REF_A}=1.0V, V_{REF_B}=V_{EN}=1.8V		16		Ω

Notes: 1. All typical values are at T_A=25°C.
2. Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

■ SWITCHING CHARACTERISTICS

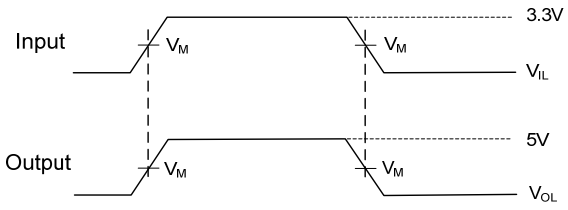
PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay From Input (A or B) to Output (B or A)	Down	t_{PLH}	V_{REF_A}=2.3V, V_{REF_B}=3.3V, V_{IH}=3.3V, V_{IL}=0, V_M=1.15V	C_L=50pF		1.7		ns
				C_L=15pF		1.4		ns
			V_{REF_A}=1.5V, V_{REF_B}=2.5V, V_{IH}=2.5V, V_{IL}=0, V_M=0.75V	C_L=50pF		1.6		ns
				C_L=15pF		1.5		ns
	Up		V_{REF_A}=2.3V, V_{REF_B}=3.3V, V_{IH}=2.3V, V_{IL}=0, V_T=3.3V, V_M=1.15V, R_L=300Ω	C_L=50pF		1.7		ns
				C_L=15pF		1.6		ns
			V_{REF_A}=1.5V, V_{REF_B}=2.5V, V_{IH}=2.5V, V_{IL}=0, V_T=2.5V, V_M=0.75V, R_L=300Ω	C_L=50pF		2		ns
				C_L=15pF		1.9		ns
Propagation Delay From Input (A or B) to Output (B or A)	Down	t_{PHL}	V_{REF_A}=2.3V, V_{REF_B}=3.3V, V_{IH}=3.3V, V_{IL}=0, V_M=1.15V	C_L=50pF		7.7		ns
				C_L=15pF		4.6		ns
			V_{REF_A}=1.5V, V_{REF_B}=2.5V, V_{IH}=2.5V, V_{IL}=0, V_M=0.75V	C_L=50pF		5.2		ns
				C_L=15pF		5.1		ns
	Up		V_{REF_A}=2.3V, V_{REF_B}=3.3V, V_{IH}=2.3V, V_{IL}=0, V_T=3.3V, V_M=1.15V, R_L=300Ω	C_L=50pF		6.8		ns
				C_L=15pF		6.5		ns
			V_{REF_A}=1.5V, V_{REF_B}=2.5V, V_{IH}=2.5V, V_{IL}=0, V_T=2.5V, V_M=0.75V, R_L=300Ω	C_L=50pF		5.3		ns
				C_L=15pF		5.2		ns

■ TEST CIRCUIT AND WAVEFORMS

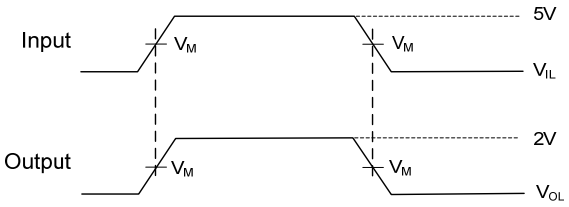


USAGE	SWITCH
Translating Up	S1
Translating Down	S2

LOAD CIRCUIT



TRANSLATING UP



TRANSLATING DOWN

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
3.The outputs are measured one at a time, with one transition per measurement.

■ DEVICE FUNCTIONAL MODES

For each channel (n), when either the An or Bn port is LOW, the switch provides a low impedance path between the An and Bn ports; the corresponding Bn or An port will be pulled LOW. The low R_{ON} of the switch allows connections to be made with minimal propagation delay and signal distortion.

When the signal is being driven from A to B and the An port is HIGH, the switch will be OFF and the Bn port will then driven to a voltage higher than V_{REF_A} by the pullup resistor that is connected to the pull-up supply voltage (V_{PU}#). This functionality allows seamless translation between higher and lower voltages selected by the user, without the need for directional control.

Refer to Function table for a summary of device operation. For additional details on the functional operation of the UTC **ULSF0102** family of devices, see the Down Translation with the UTC **ULSF0102** Family and Up Translation with the UTC **ULSF0102** Family videos.

Table 1. Device Functionality

Signal Direction (Note 1)	Input State	Switch State	Functionality
A TO B (Up Translation)	A=LOW	ON (Low Impedance)	B-side voltage is pulled low through the switch to the A-side voltage
	A=HIGH	OFF (High Impedance)	B-side voltage is clamped at V_{REF_A} and then pulled up to the V_{PU} # supply voltage

Note: The downstream channel should not be actively driven through a low impedance driver, or else there may be bus contention.

■ TYPICAL APPLICATIONS

The UTC **ULSF0102** family has an EN input that is used to disable the device by setting EN LOW, placing all I/Os in the high-impedance state. Since the UTC **ULSF0102** family of devices are switch-type voltage translators, the power consumption is very low. UTC recommends always enabling the UTC **ULSF0102** family for bidirectional applications (I^2C, SMBus, PMBus, or MDIO).

Table 2. Application Operating Condition

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Voltage A (Note 1)	V_{REF_A}		0.95		4.5	V
Reference Voltage B	V_{REF_B}		V_{REF_A} +0.8		5.5	V
Input Voltage on EN Pin	$V_{I(EN)}$		V_{REF_A} +0.8		5.5	V
Pull-Up Supply Voltage	V_{PU}		0		V_{REF_B}	V

Note: V_{REF_A} is required to be the lowest voltage level across all inputs and outputs.

The 200 kΩ, pull-up resistor is required to allow V_{REF_B} to regulate the EN input and properly bias the device for translation. A filter capacitor on V_{REF_B} is recommended. Also V_{REF_B} and $V_{I(EN)}$ are recommended to be 1.0V higher than V_{REF_A} for best signal integrity.

■ TYPICAL APPLICATIONS (Cont.)

Bidirectional Translation

For the bidirectional translation configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{REF_B} and both pins must be pulled up to the HIGH side V_{PU} through a pull-up resistor (typically 200 kΩ). This allows V_{REF_B} to regulate the EN input and bias the channels for proper translation. A filter capacitor on V_{REF_B} is recommended for a stable supply at the device. The controller output driver can be push-pull or open-drain (pull-up resistors may be required) and the peripheral device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to V_{PU}).

If either output is push-pull, data must be unidirectional or the outputs must be tri-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW bus contention in either

direction. If both outputs are open-drain, no direction control is needed.

When V_{REF_B} is connected through a 200kΩ resistor to a 3.3V V_{PU} power supply and V_{REF_A} is set 1.8 V, as shown in Figure Figure 1, the A1 and A2 channels have a maximum output voltage equal to V_{REF_A}, and the B1 and B2 channels have has a maximum output voltage equal to V_{PU}.

Pull-up Resistor Sizing

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15mA. This ensures a voltage drop of 260mV to 350mV to have a valid LOW signal on the downstream channel. If the current through the pass transistor is higher than 15mA, the voltage drop is also higher in the ON state. To set the current through each pass transistor at 15mA, calculate the pull-up resistor value using the following equation:

$$R_{PU} = (V_{PU} – 0.35V) / 0.015A \quad (1)$$

Table 3 summarizes resistor values, reference voltages, and currents at 15mA, 10mA, and 3mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the voltage drop across the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the UTC **ULSF0102** family device at 0.175V, although the 15mA applies only to current flowing through the UTC **ULSF0102** family device.

Table 3. Pull-up Resistor Values

V_{DPU} (Note1, 2)	15mA		10mA		3mA	
	NOMINAL(Ω)	+10%(Ω) (Note 3)	NOMINAL(Ω)	+10%(Ω) (Note 3)	NOMINAL(Ω)	+10%(Ω) (Note 3)
5V	310	341	465	512	1550	1705
3.3V	197	217	295	325	983	1082
2.5V	143	158	215	237	717	788
1.8V	97	106	145	160	483	532
1.5V	77	85	115	127	383	422
1.2V	57	63	85	94	283	312

Notes: 1. Calculated for V_{OL}=0.35V.

2. Assumes output driver V_{OL}=0.175V at stated current.

3. +10% to compensate for V_{DD} range and resistor tolerance.

■ TYPICAL APPLICATION CIRCUIT

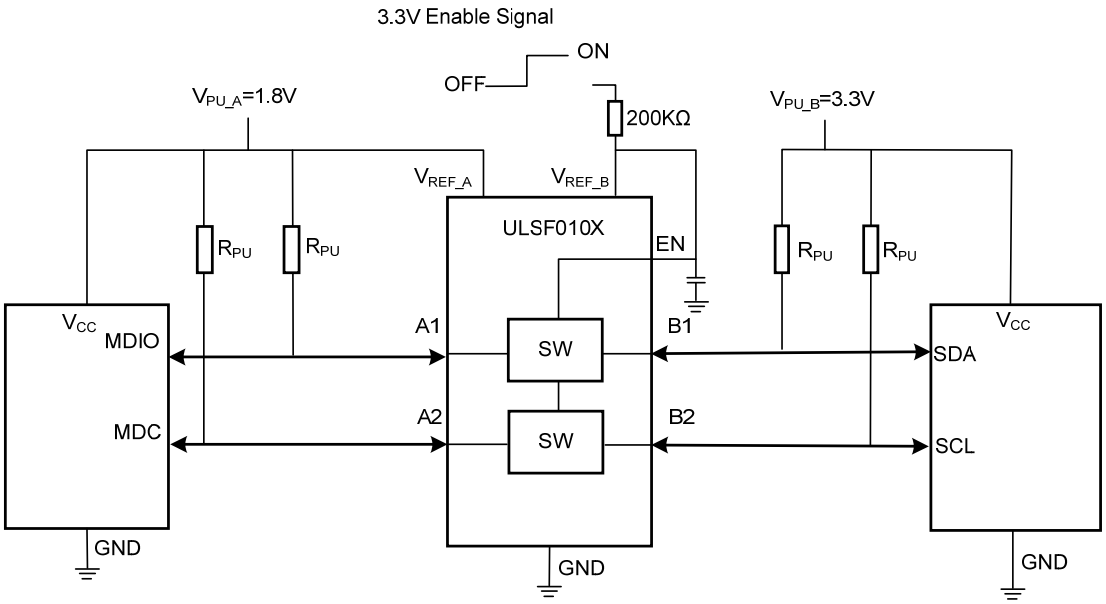


Figure 1. Typical Application Circuit for Open-Drain Translation (MDIO shown as an example)

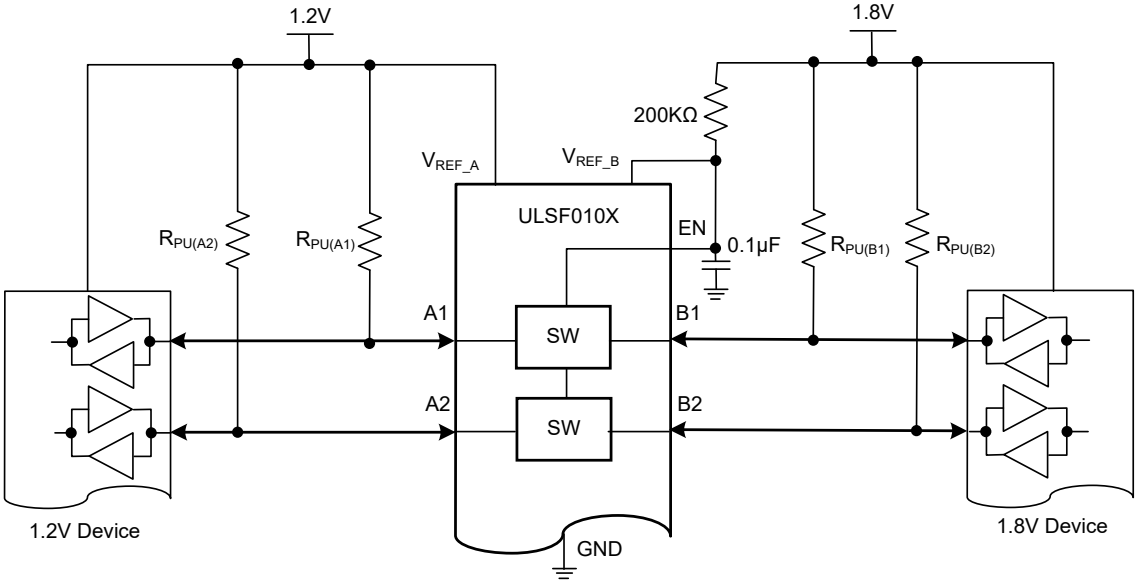


Figure 2. 1.2 to 1.8V Level Translation with ULSF010X