



UT80N055M

Preliminary

POWER MOSFET

80A, 55V N-CHANNEL POWER MOSFET

DESCRIPTION

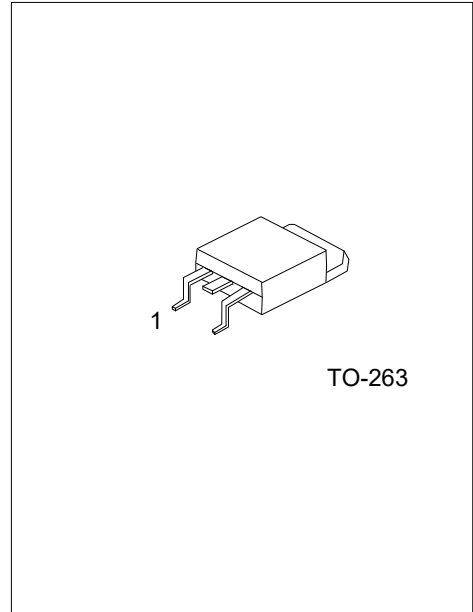
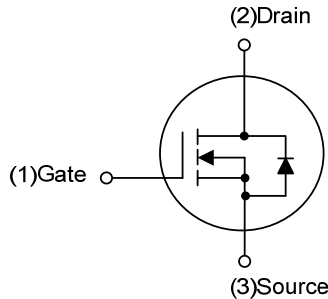
The UTC **UT80N055M** is a N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low $R_{DS(ON)}$ characteristic by high cell density trench technology.

The UTC **UT80N055M** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

FEATURES

- * $R_{DS(ON)} \leq 5.0 \text{ m}\Omega @ V_{GS}=10\text{V}, I_D=40\text{A}$
- * $R_{DS(ON)} \leq 7.0 \text{ m}\Omega @ V_{GS}=4.5\text{V}, I_D=40\text{A}$
- * Low capacitance
- * Low gate charge
- * Fast switching capability
- * Avalanche energy specified

SYMBOL



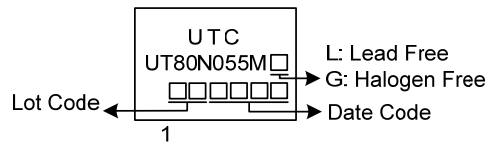
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT80N055ML-TQ2-T	UT80N055MG-TQ2-T	TO-263	G	D	S	Tube
UT80N055ML-TQ2-R	UT80N055MG-TQ2-R	TO-263	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT80N055MG-TQ2-T</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TQ2: TO-263</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATING ($T_C=25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	55	V
Gate-Source Voltage	V_{GSS}	± 20	V
Drain Current	DC	I_D	80
	Pulsed (Note 2)	I_{DM}	160
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	185
Peak Diode Recovery dv/dt (Note 4)	dv/dt	2.1	V/ns
Power Dissipation	P_D	93	W
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.1\text{mH}$, $I_{AS} = 61\text{A}$, $V_{DD} = 25\text{V}$, $R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	1.34	$^\circ\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

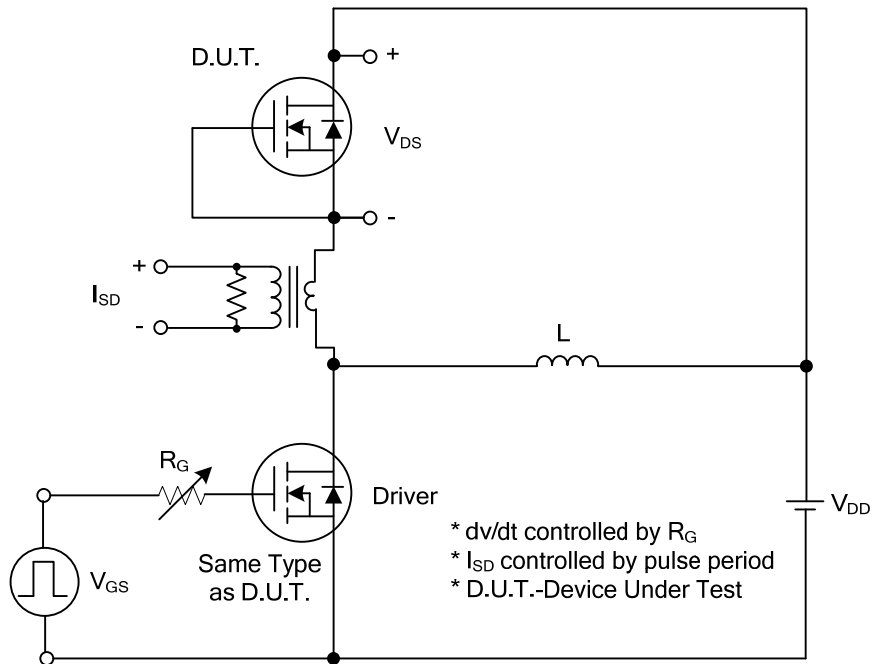
■ ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	55			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =55V, V _{GS} =0V			1	μA
Gate-Source Leakage Current	Forward	V _{GS} =+20V, V _{DS} =0V			+100	nA
	Reverse				-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =40A			5.0	mΩ
		V _{GS} = 4.5V, I _D =40A			7.0	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =25V, f=1.0MHz		5916		pF
Output Capacitance	C _{OSS}			577		pF
Reverse Transfer Capacitance	C _{RSS}			469		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{DS} =44V, V _{GS} =10V, I _D =80A (Note 1, 2)		185		nC
Gate to Source Charge	Q _{GS}			13		nC
Gate to Drain Charge	Q _{GD}			86		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =27.5V, V _{GS} =10V, I _D =80A, R _G =3Ω (Note 1, 2)		15		ns
Rise Time	t _R			17		ns
Turn-OFF Delay Time	t _{D(OFF)}			90		ns
Fall-Time	t _F			42		ns
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I _S				80	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				160	A
Diode Forward Voltage	V _{SD}	I _F =80A, V _{GS} =0V			1.4	V
Reverse Recovery Time (Note 1)	t _{rr}	I _S =30A, V _{GS} =0V, dI _F /dt = 100A/μs		98		ns
Reverse Recovery Charge	Q _{rr}			166		nC

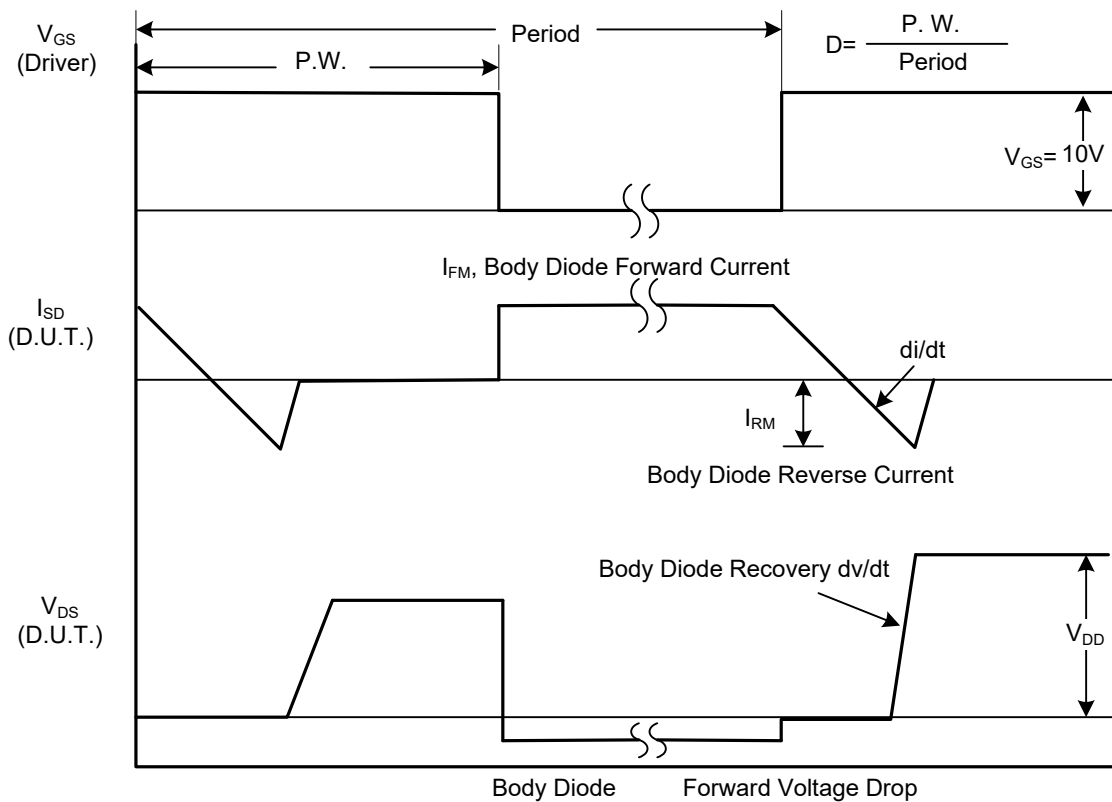
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

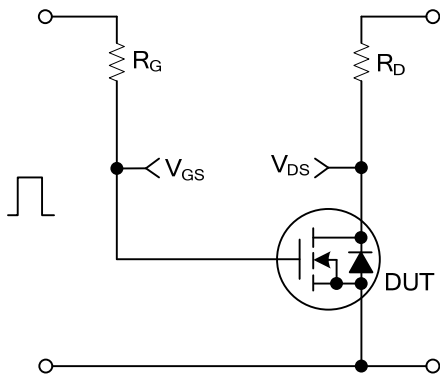


Peak Diode Recovery dv/dt Test Circuit

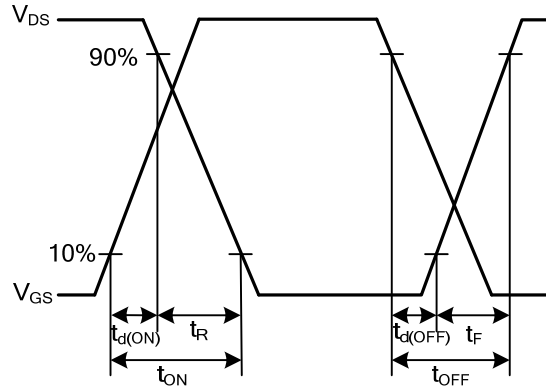


Peak Diode Recovery dv/dt Waveforms

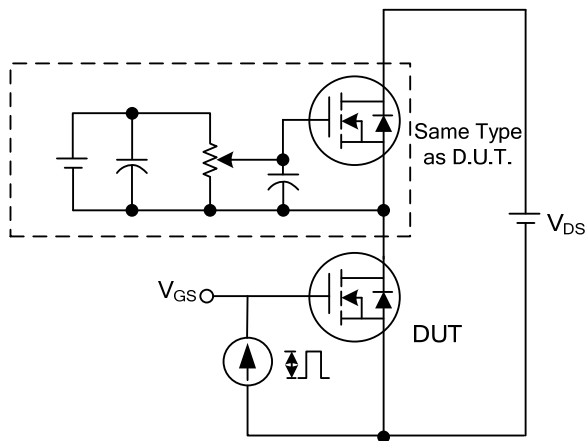
■ TEST CIRCUITS AND WAVEFORMS



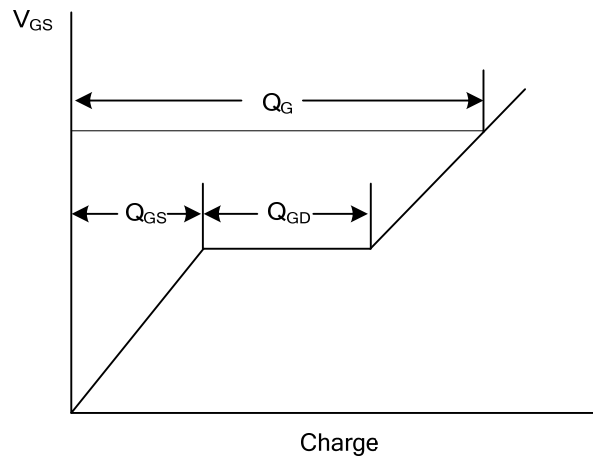
Switching Test Circuit



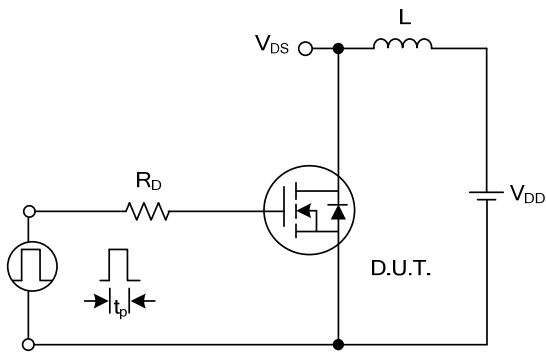
Switching Waveforms



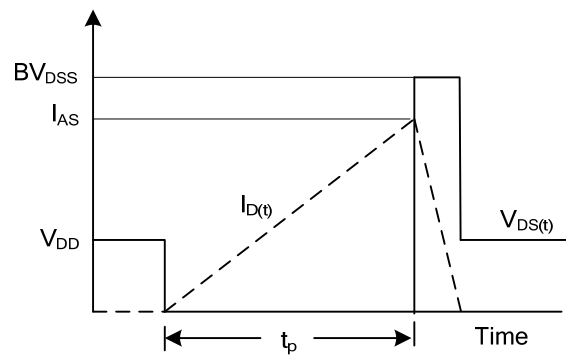
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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