



**18NM100Z**

Preliminary

**POWER MOSFET**

**18A, 1000V N-CHANNEL SUPER-JUNCTION MOSFET**

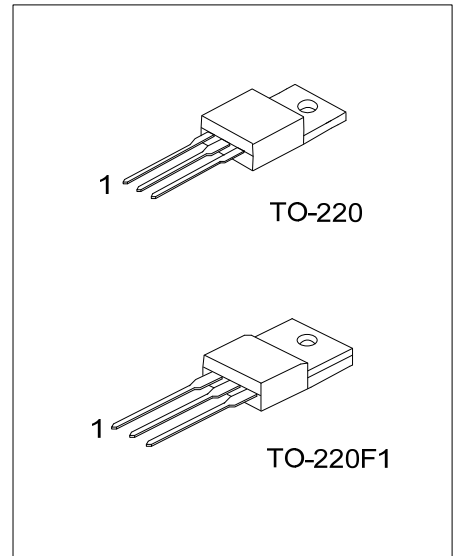
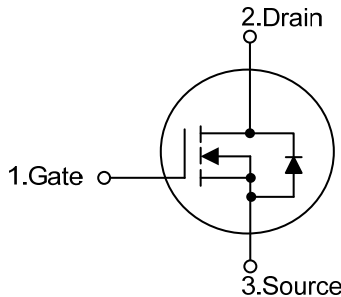
■ DESCRIPTION

The UTC **18NM100Z** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at AC-DC converters for power applications.

■ FEATURES

- \*  $R_{DS(ON)} \leq 0.45 \Omega @ V_{GS}=10V, I_D=9.0A$
- \* Fast switching capability
- \* Avalanche energy tested
- \* Improved dv/dt capability, high ruggedness
- \* With ESD protection

■ SYMBOL



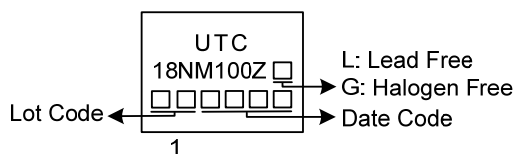
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
18NM100Z L-TN3-R	18NM100ZG-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>18NM100ZG-TN3-R</p>	<p>(1) R: Tape Reel</p> <p>(2) TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATING ( $T_C=25^\circ\text{C}$  unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	1000	V
Gate-Source Voltage		$V_{GSS}$	$\pm 20$	V
Drain Current	DC	$I_D$	18	A
	Pulsed (Note 2)	$I_{DM}$	54	A
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	650	mJ
Peak Diode Recovery $dv/dt$ (Note 4)		$dv/dt$	0.97	V/ns
Power Dissipation	TO-220	$P_D$	125	W
	TO-220F1		34	W
Junction Temperature		$T_J$	+150	$^\circ\text{C}$
Storage Temperature Range		$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $L = 100\text{mH}$ ,  $I_{AS} = 3.6\text{A}$ ,  $V_{DD} = 50\text{V}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$ .

4.  $I_{SD} \leq 18\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$ .

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		$\theta_{JA}$	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	TO-220	$\theta_{JC}$	1	$^\circ\text{C}/\text{W}$
	TO-220F1		3.6	$^\circ\text{C}/\text{W}$

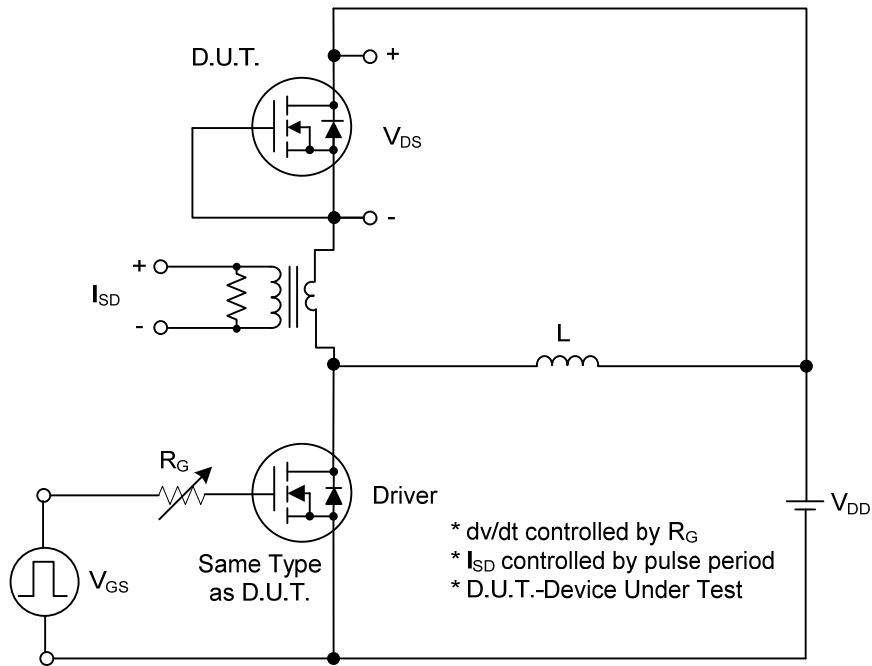
■ ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	1000			V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =1000V, V <sub>GS</sub> =0V			10	μA
Gate-Source Leakage Current	Forward	I <sub>GSS</sub> V <sub>GS</sub> =+20V, V <sub>DS</sub> =0V			+10	μA
	Reverse		V <sub>GS</sub> =-20V, V <sub>DS</sub> =0V			-10
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.5		4.5	V
Static Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =9.0A			0.45	Ω
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =50V, f=1.0MHz		1600		pF
Output Capacitance	C <sub>OSS</sub>			96		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			3		pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge	Q <sub>G</sub>	V <sub>DS</sub> =760V, V <sub>GS</sub> =10V, I <sub>D</sub> =18A (Note 1, 2)		45		nC
Gate to Source Charge	Q <sub>GS</sub>			12		nC
Gate to Drain Charge	Q <sub>GD</sub>			11		nC
Turn-ON Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =100V, V <sub>GS</sub> =10V, I <sub>D</sub> =18A, R <sub>G</sub> =25Ω (Note 1, 2)		16		ns
Rise Time	t <sub>r</sub>			22		ns
Turn-OFF Delay Time	t <sub>D(OFF)</sub>			120		ns
Fall-Time	t <sub>f</sub>			53		ns
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Continuous Drain-Source Diode Forward Current	I <sub>S</sub>				18	A
Maximum Pulsed Drain-Source Diode Forward Current	I <sub>SM</sub>				54	A
Diode Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> =18A, V <sub>GS</sub> =0V			1.4	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>S</sub> =18A, V <sub>GS</sub> =0V, dI <sub>F</sub> /dt = 100 A/μs		560		ns
Reverse Recovery Charge (Note 1)	Q <sub>rr</sub>				11.3	

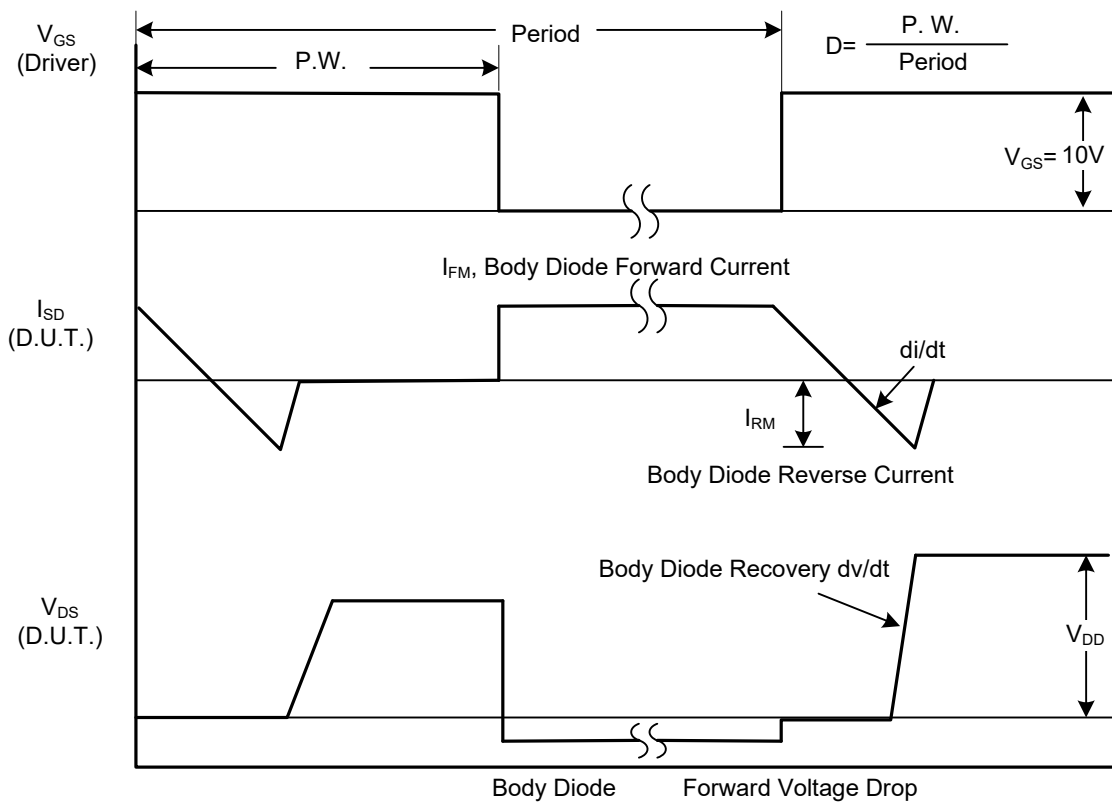
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

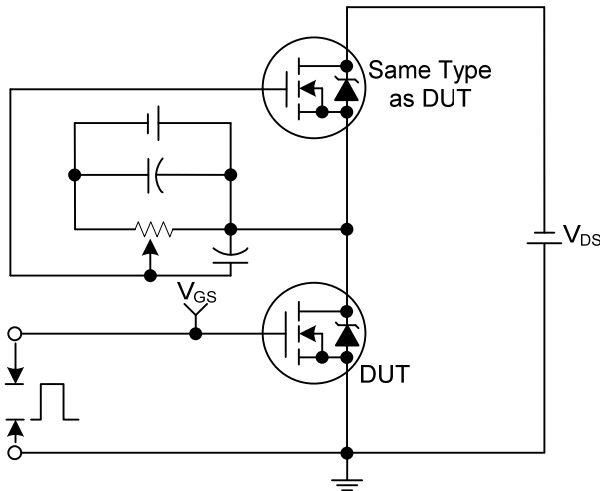


Peak Diode Recovery dv/dt Test Circuit

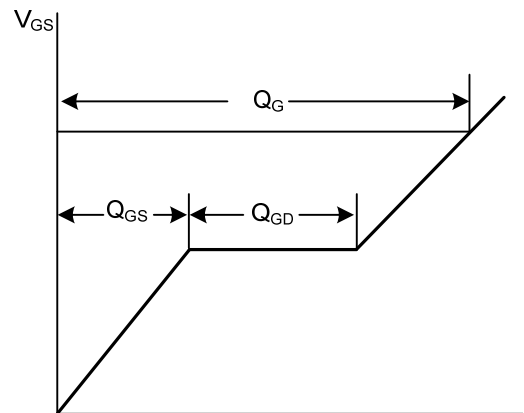


Peak Diode Recovery dv/dt Waveforms

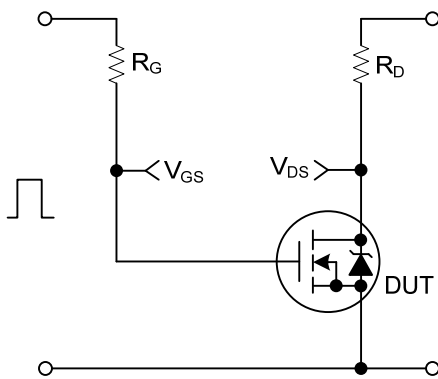
■ TEST CIRCUITS AND WAVEFORMS



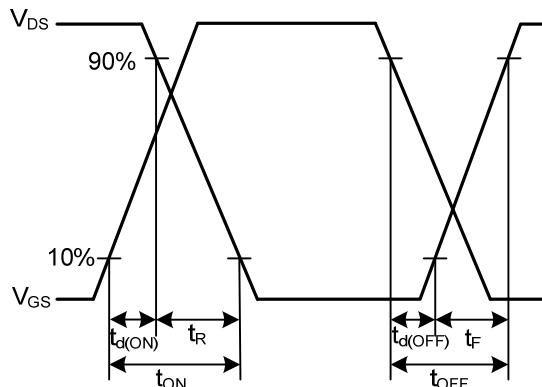
Gate Charge Test Circuit



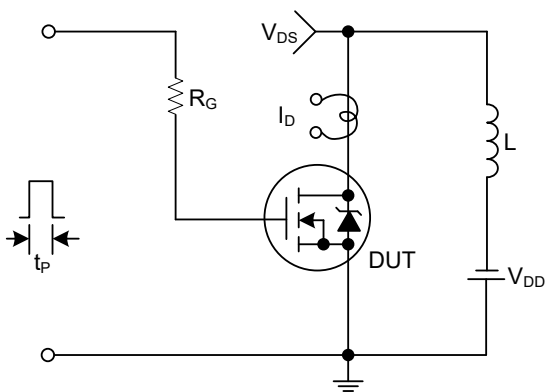
Gate Charge Waveforms



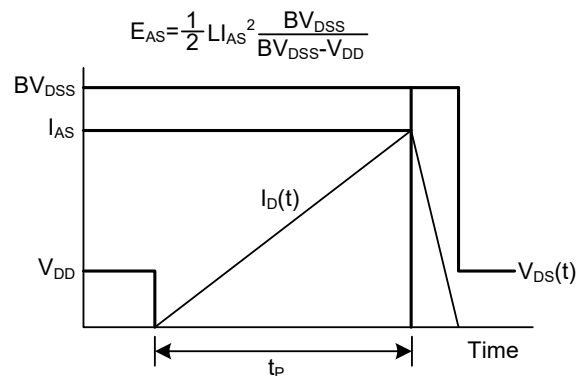
Resistive Switching Test Circuit



Resistive Switching Waveforms



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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