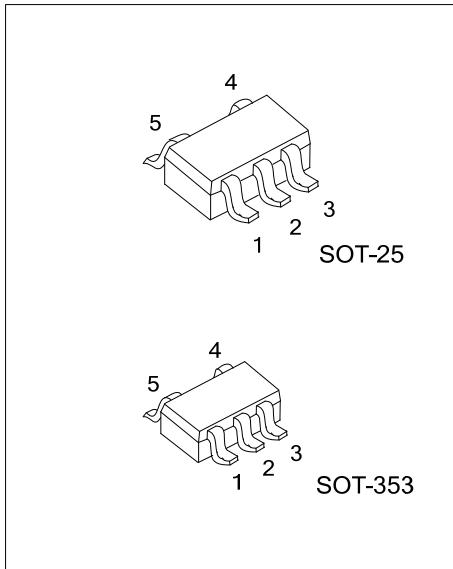


SINGLE POWER SUPPLY SINGLE INVERTER GATE CMOS LOGIC LEVEL SHIFTER

■ DESCRIPTION

The **U74LV1T04** is a single, level translating inverter gate. The low threshold inputs support 1.8V input logic at $V_{cc}=3.3V$ and can be used in 1.8V to 3.3V level up translation. In addition, the 5V tolerant input pins enable level down translation (3.3V to 2.5V output at $V_{cc}=2.5V$). The output level is referenced to the supply Voltage and supports 1.8V, 2.5V, 3.3V and 5.0V CMOS levels.

The wide V_{cc} range permits the generation of output levels to connect to controllers or processors.



■ FEATURES

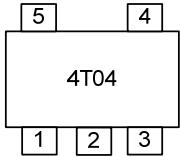
- * Single supply voltage translator at 1.8V, 2.5V, 3.3V and 5.0V
- * Low Power Current: $I_{cc}=10\mu A$ (Max.)
- * $\pm 8mA$ Output Drive ($V_{cc}=5.0V$)

■ ORDERING INFORMATION

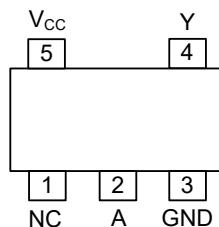
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LV1T04L-AF5-R	U74LV1T04G-AF5-R	SOT-25	Tape Reel
U74LV1T04L-AL5-R	U74LV1T04G-AL5-R	SOT-353	Tape Reel

U74LV1T04G-AF5-R 	(1)R: Tape Reel (2)AF5: SOT-25, AL5: SOT-353 (3)G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING



■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	NC	Not Connected
2	A	Input A
3	GND	Ground
4	Y	Output Y
5	V _{CC}	Positive supply

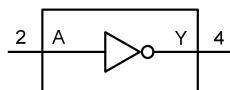
Note: I=Input, O=Output, I/O= Input or Output, G=Ground, P=Power

■ FUNCTION TABLE (each gate)

INPUT (Lower Level Input)	OUTPUT (V _{CC} CMOS)
A	Y
H	L
L	H

Notes: 1. H = HIGH Voltage Level; L = LOW Voltage Level

■ LOGIC DIAGRAM (positive logic)

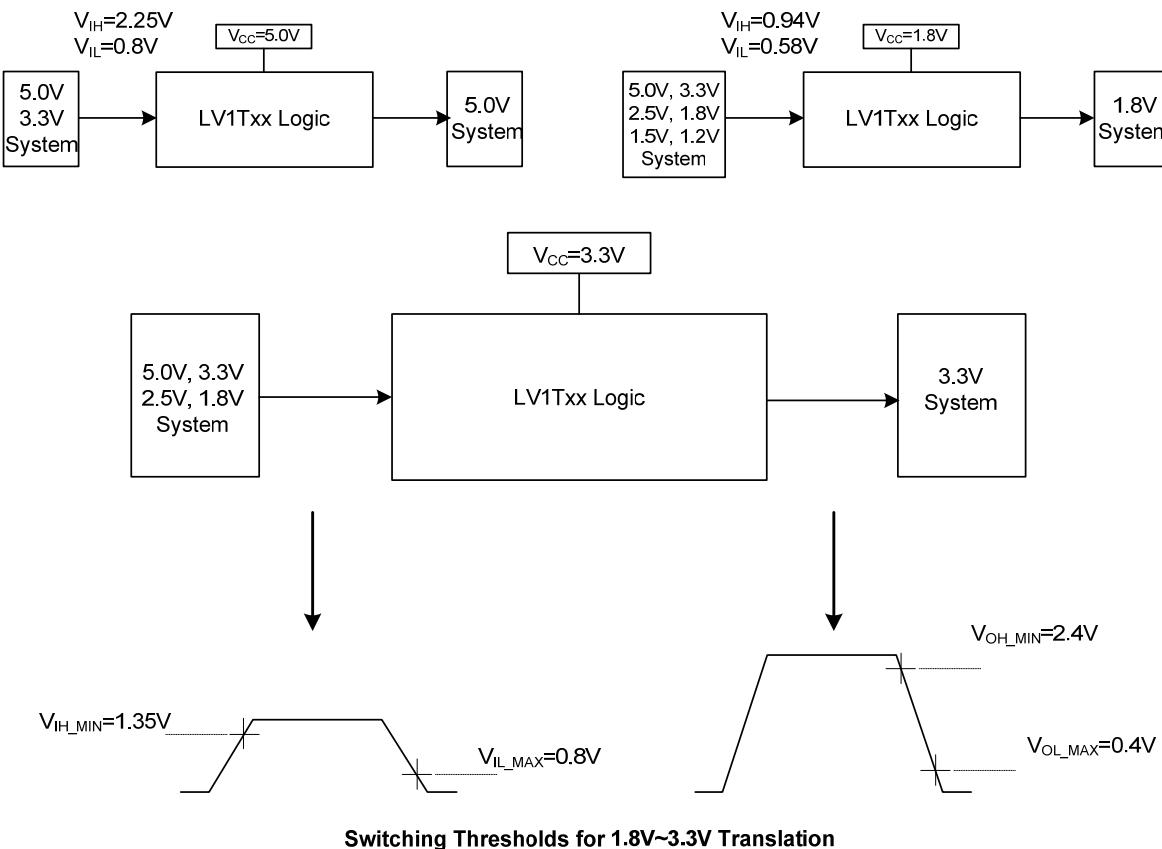


Logic Symbol



IEC Logic Symbol

- TYPICAL DESIGN EXAMPLES



ABSOLUTE MAXIMUM RATING ($T_A=25^\circ\text{C}$, unless otherwise specified) (Note 2)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 7	V
Input Voltage (Note 2)	V_{IN}		-0.5 ~ 7	V
Output Voltage (Note 2)	V_{OUT}	Output HIGH or LOW state	-0.5 ~ $V_{CC}+0.5$	V
		Output in power-off state	-0.5 ~ 4.6	V
Continuous Output Current			± 25	mA
Continuous current through V_{CC} or GND			± 50	mA
Input Clamp Current	I_{IK}	$V_{IN}<0$	-20	mA
Output Clamp Current	I_{OK}	$V_{OUT}<0$ or $V_{OUT}>V_{CC}$	± 20	mA
Junction Temperature	T_J		+150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}		-65 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.6		5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC}=1.8\text{V}$			20	ns/V
		$V_{CC}=3.3\text{V}$ or 2.5V			20	ns/V
		$V_{CC}=5\text{V}$			20	ns/V
Operating Temperature	T_A		-40		+125	$^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL		RATINGS	UNIT
Junction to Ambient	SOT-25	θ_{JA}	230	$^\circ\text{C}/\text{W}$
	SOT-353		350	$^\circ\text{C}/\text{W}$

■ STATIC CHARACTERISTICS ($T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC}=1.65V \sim 1.8V$	0.94			V
		$V_{CC}=2.0V$	1.02			V
		$V_{CC}=2.25V \sim 2.5V$	1.135			V
		$V_{CC}=2.75V$	1.21			V
		$V_{CC}=3.0V \sim 3.3V$	1.35			V
		$V_{CC}=3.6V$	1.47			V
		$V_{CC}=4.5V \sim 5.0V$	2.25			V
		$V_{CC}=5.5V$	2.5			V
Low-Level Input Voltage	V_{IL}	$V_{CC}=1.65V \sim 2V$		0.58		V
		$V_{CC}=2.25V \sim 2.75V$		0.75		V
		$V_{CC}=3V \sim 3.6V$		0.8		V
		$V_{CC}=4.5V \sim 5.5V$		0.8		V
High-Level Output Voltage	V_{OH}	$V_{CC}=1.65V \sim 5.5V, I_{OH}=-20\mu A$	$V_{CC}-0.1$			V
		$V_{CC}=1.65V$	1.28			V
		$V_{CC}=1.8V$	1.5			V
		$V_{CC}=2.3V$	2			V
		$I_{OH}=-2.3mA$	2			V
		$V_{CC}=2.5V, I_{OH}=-3mA$	2.25			V
		$V_{CC}=3V$	2.78			V
		$I_{OH}=-5.5mA$	2.6			V
		$V_{CC}=3.3V, I_{OH}=-5.5mA$	2.9			V
		$V_{CC}=4.5V$	4.2			V
		$I_{OH}=-4mA$	4.1			V
		$V_{CC}=5V, I_{OH}=-8mA$	4.6			V
Low-Level Output Voltage	V_{OL}	$V_{CC}=1.65V \sim 5.5V, I_{OL}=20\mu A$		0.1		V
		$V_{CC}=1.65V, I_{OL}=1.9mA$		0.2		V
		$V_{CC}=2.3V$	$I_{OL}=2.3mA$	0.1		V
		$I_{OL}=3mA$		0.15		V
		$V_{CC}=3V$	$I_{OL}=3mA$	0.1		V
		$I_{OL}=5.5mA$		0.2		V
		$V_{CC}=4.5V$	$I_{OL}=4mA$	0.15		V
		$I_{OL}=8mA$		0.3		V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0V, 1.8V, 2.5V, 3.3V, 5.5V, V_{IN}=0V$ or V_{CC}		0.12		μA
Quiescent Supply Current	I_Q	$V_{CC}=1.8V, 2.5V, 3.3V, 5V, V_{IN}=0V$ or V_{CC} , $I_o=0$; Open on loading		1		μA
Additional Quiescent Supply Current	ΔI_Q	$V_{CC}=5.5V$, one input at 0.3V or 3.4V, other inputs at 0 or V_{CC} , $I_o=0$		1.35		mA
		$V_{CC}=1.8V$, one input at 0.3V or 1.1V, other inputs at 0 or V_{CC} , $I_o=0$		10		μA
Input Capacitance	C_{IN}	$V_{CC}=3.3V, V_{IN}=V_{CC}$ or GND	2			pF
Output Capacitance	C_{OUT}	$V_{CC}=3.3V, V_{OUT}=V_{CC}$ or GND	2.5			pF

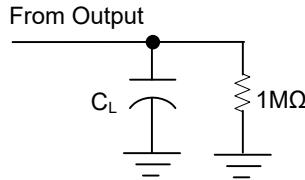
■ DYNAMIC CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input (Any In) to output(Y)	t_{PLH} / t_{PHL}	$C_L=15\text{pF}$	$V_{CC}=1.8\text{V}$	10.5	11	ns
			$V_{CC}=2.5\text{V}$	6.0	6.5	ns
			$V_{CC}=3.3\text{V}$	4.8	6.0	ns
			$V_{CC}=5\text{V}$	4.0	6.0	ns
		$C_L=30\text{pF}$	$V_{CC}=1.8\text{V}$	12	13	ns
			$V_{CC}=2.5\text{V}$	6.5	7.5	ns
			$V_{CC}=3.3\text{V}$	5.5	7.0	ns
			$V_{CC}=5\text{V}$	5.0	7.0	ns

■ OPERATING CHARACTERISTICS ($f=1\text{MHz} & 10\text{MHz}$, $T_A=25^\circ\text{C}$, unless otherwise specified)

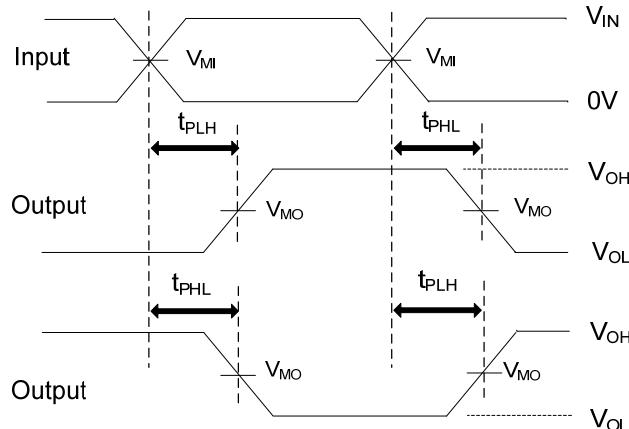
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	$V_{CC}=1.8\text{V}\pm0.15\text{V}$		10		pF
		$V_{CC}=2.5\text{V}\pm0.2\text{V}$		10		pF
		$V_{CC}=3.3\text{V}\pm0.3\text{V}$		10		pF
		$V_{CC}=5\text{V}\pm0.5\text{V}$		10		pF

■ TEST CIRCUIT AND WAVEFORMS



	$V_{CC}=2.5\text{V}\pm 0.2\text{V}$	$V_{CC}=3.3\text{V}\pm 0.3\text{V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_{MI}	$V_I/2$	$V_I/2$
V_{MO}	$V_{CC}/2$	$V_{CC}/2$

TEST CIRCUIT



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

- Notes:
1. C_L includes probe and jig capacitance
 2. All input pulses are supplied by generators having the following characteristics: $P_{RR} \leq 10\text{MHz}$, $Z_0=50\text{W}$, slew rate $\geq 1\text{V/ns}$.
 3. The outputs are measured one at a time, with one transition per measurement.
 4. t_{PLH} and t_{PHL} are the same as t_{PD} .

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