



UFB4332

Preliminary

POWER MOSFET

60A, 250V N-CHANNEL ENHANCEMENT MODE TRENCH POWER MOSFET

DESCRIPTION

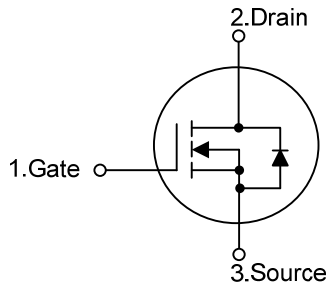
The UTC **UFB4332** is an N-channel Power MOSFET, it uses UTC's advanced technology to provide the customers with low voltage inverter applications.

The UTC **UFB4332** is suitable for high efficiency synchronous rectification in SMPS, UPS, hard switched and high frequency circuits.

FEATURES

- * $R_{DS(ON)} \leq 33 \text{ m}\Omega @ V_{GS}=10V, I_D=35A$
- * High Cell Density Trench Technology
- * High Power and Current Handling Capability

SYMBOL

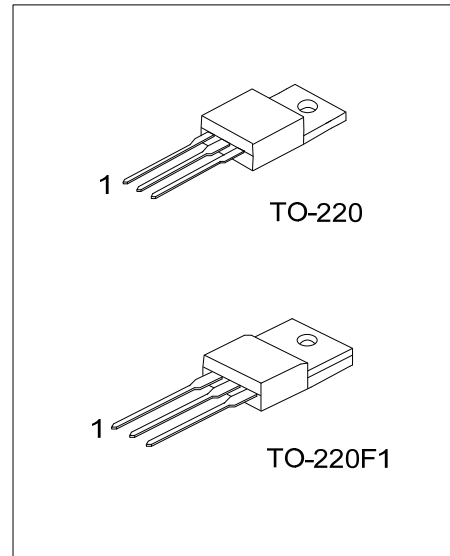


ORDERING INFORMATION

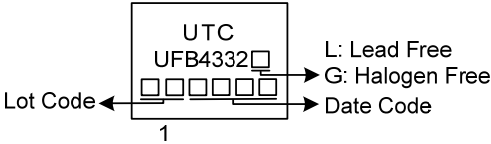
Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UFB4332L-TA3-T	UFB4332G-TA3-T	TO-220	G	D	S	Tube
UFB4332L-TF1-T	UFB4332G-TF1-T	TO-220F1	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UFB4332G-TA3-T</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Green Package</p>	<p>(1) T: Tube</p> <p>(2) TA3: TO-220, TF1: TO-220F1</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	250	V
Gate-Source Voltage		V_{GSS}	± 20	V
Continuous Drain Current	Continuous	I_D	60	A
Pulsed Drain Current	Pulsed (Note 2)	I_{DM}	120	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	655	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.47	V/mS
Power Dissipation	TO-220	P_D	150	W
	TO-220F1		57	W
Junction Temperature		T_J	+250	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +250	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 0.39\text{mH}$, $I_{AS} = 58\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	TO-220	θ_{JC}	0.83	$^\circ\text{C}/\text{W}$
	TO-220F1		2.19	$^\circ\text{C}/\text{W}$

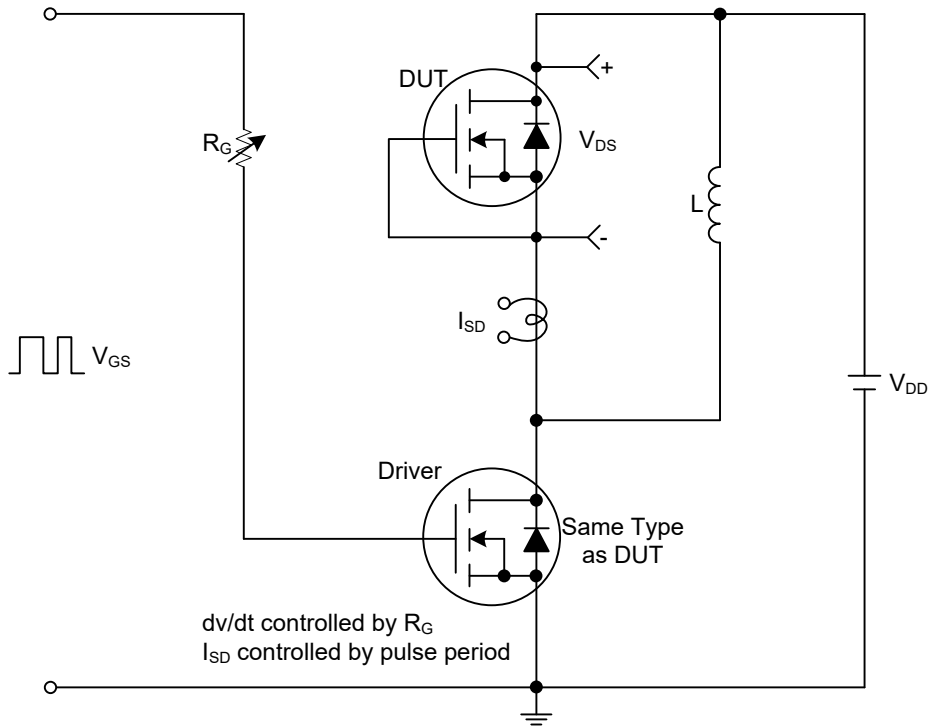
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	250			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =250V, V _{GS} =0V			10	μA
Gate- Source Leakage Current	Forward	I _{GSS} V _{GS} =20V, V _{DS} =0V V _{GS} =-20V, V _{DS} =0V			100	nA
	Reverse				-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} =V _{GS} , I _D =250μA	3.0		5.0	V
Static Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =35A			33	mΩ
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		14.16		nF
Output Capacitance	C _{OSS}			566		pF
Reverse Transfer Capacitance	C _{RSS}			438		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge (Note 1)	Q _G	V _{DS} =200V, V _{GS} =10V, I _D =60A (Note 1, 2)		282		nC
Gate-Source Charge	Q _{GS}			140		nC
Gate-Drain Charge	Q _{GD}			111		nC
Turn-On Delay Time (Note 1)	t _{D(ON)}	V _{DS} =100V, V _{GS} =10V, I _D =60A, R _G =3.3Ω (Note 1, 2)		64		ns
Turn-On Rise Time	t _R			45.85		ns
Turn-Off Delay Time	t _{D(OFF)}			92.6		ns
Turn-Off Fall Time	t _F			48.3		ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Maximum Body-Diode Continuous Current	I _S				60	A
Maximum Body-Diode Pulsed Current	I _{SM}				120	A
Drain-Source Diode Forward Voltage (Note 1)	V _{SD}	I _S =60A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t _{rr}	I _S =30A, V _{GS} =0V,		262		ns
Body Diode Reverse Recovery Charge	Q _{rr}	dI _F /dt=100A/μs		1932		nC

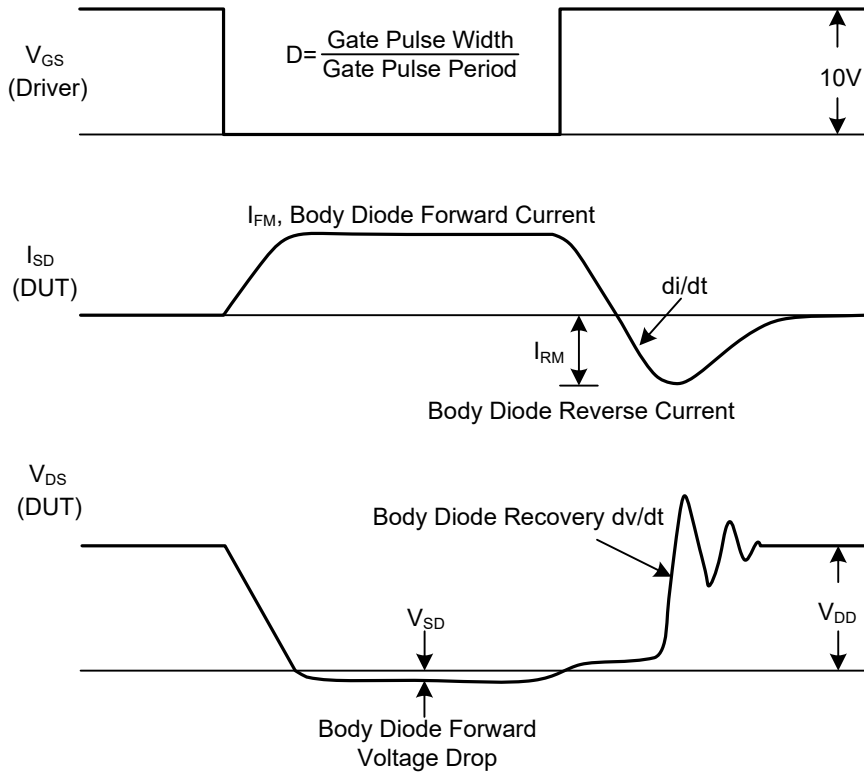
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS



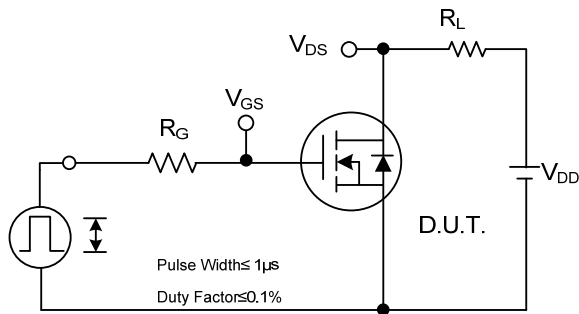
Peak Diode Recovery dv/dt Test Circuit



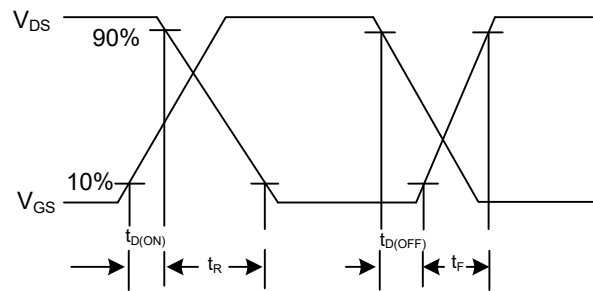
Peak Diode Recovery dv/dt Test Circuit and Waveforms

Peak Diode Recovery dv/dt Waveforms

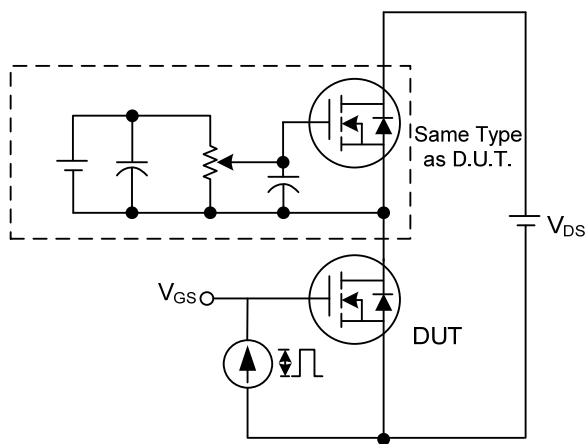
■ TEST CIRCUITS AND WAVEFORMS



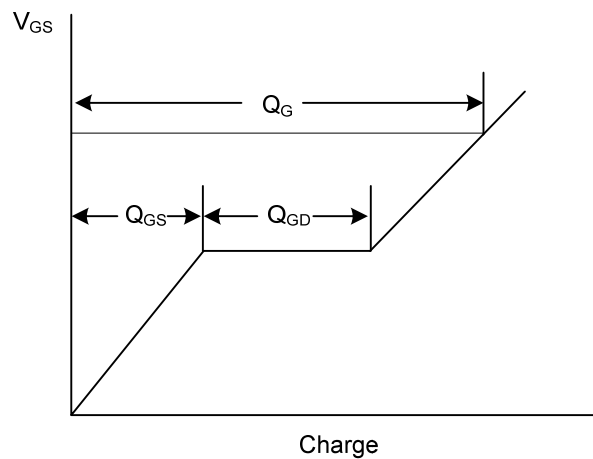
Switching Test Circuit



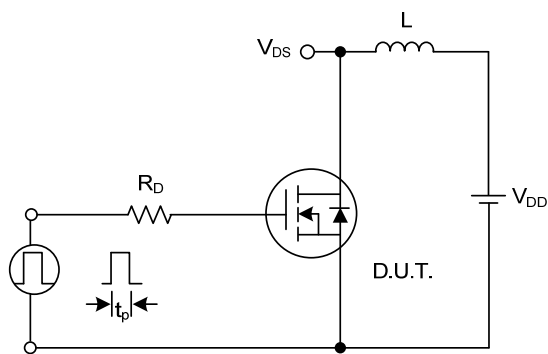
Switching Waveforms



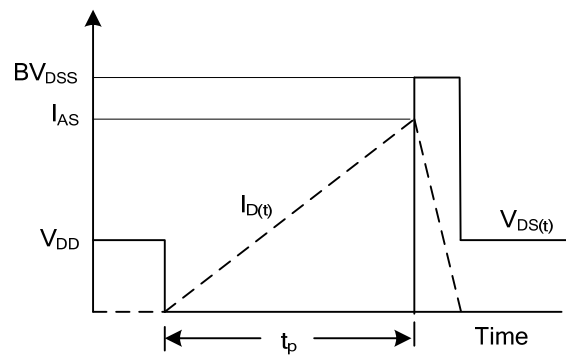
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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