RESET TIMER IC FOR MOBILE EQUIPMENTS

DFN2020-8

■ DESCRIPTION

The UTC **UIC832** is a reset timer IC for mobile equipment which require long interval for reset sequence. The long interval prevents unexpected resets caused by accidental key operations.

When both active-low input pins (SR0 and SR1) are activated at the same time, the UTC **UIC832** will generate reset signals after output delay time.

UTC **UIC832X-Q, UIC832B-R**, or UTC **UIC832X-T**:

A reset signal will be released automatically after output release time or by making one of the active-low input pins high, a reset signal can be released before output release time.

Output delay time is fixed.

The UTC **UIC832** provides ultra-low supply current while a reset signal is remaining active or after being sent out.

■ FEATURES

* Operating Voltage Range (Maximum Rating): 1.65V ~ 5.5V (6V)
* Supply Current 1 (at standby): Typ. 0.55μA (V_{DD} = 5.5V)
* Supply Current 2 (at active before reset signal output): Typ. 1.2μA (V_{DD} = 5.5V)
* Supply Current 3 (at active after reset signal output): Typ. 0.15μA (V_{DD} = 5.5V)
* Operating Temperature Range: -40 ~+85°C
* Output Delay Time(UIC832X-Q): Typ. 7.5s
  (UIC832B-R): Typ. 10s
  (UIC832X-T): Typ. 3.0s
* Output Delay Time Accuracy: ±10%
* Output Release Time (UIC832X-Q): Typ. 0.234s
  (UIC832B-R): Typ. 0.313s
  (UIC832X-T): Typ. 0.1875s
* Output Release Time Accuracy: ±10%
* Output Type (UIC832A): N-Channel Open Drain
  (UIC832B): N-Channel Open Drain and CMOS

■ ORDERING INFORMATION

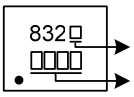
Ordering Number		Output Configuration				Package	Packing
Lead Free	Halogen Free	Output Delay Time	Output Release Time	Unit	Code		
UIC832AL-x-K08-2020-R	UIC832AG-x-K08-2020-R	7.5	0.234	s	Q	DFN2020-8	Tape Reel
		10	0.313	s	R		
UIC832BL-x-K08-2020-R	UIC832BG-x-K08-2020-R	3.0	0.1875	s	T		

Note: Q, R, T: A reset signal will be released automatically after output release time.
A reset signal can be released before output release time by making one of the active-low input pins high.
Refer to the above table for the output delay time and the output release time for each device.

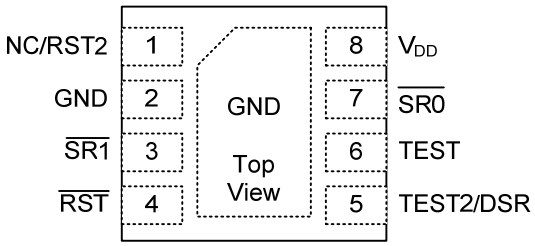
UIC832XG-x-K08-2020-R

(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) K08-2020: DFN2020-8
(3)Output Time Configuration	(3) Refer to Output Delay Time and Output Release Time
(4)Green Package	(4) G: Halogen Free and Lead Free, L: Lead Free
(5)Output Configuration	(5) A: N-Channel Open Drain B: N-Channel Open Drain and COMS

■ MARKING



■ PIN CONFIGURATION

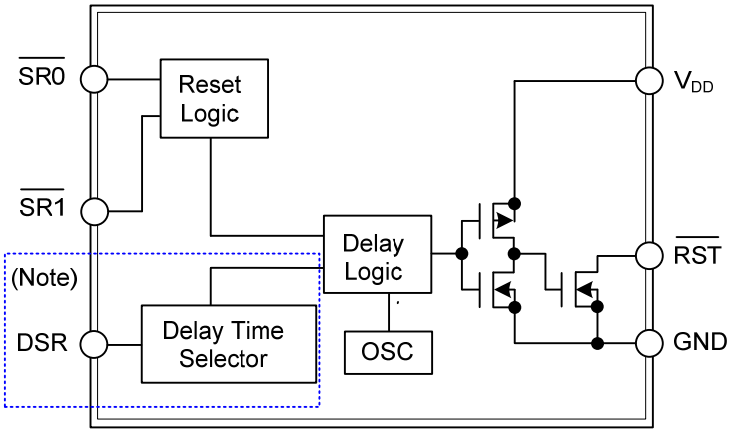


■ PIN DESCRIPTION

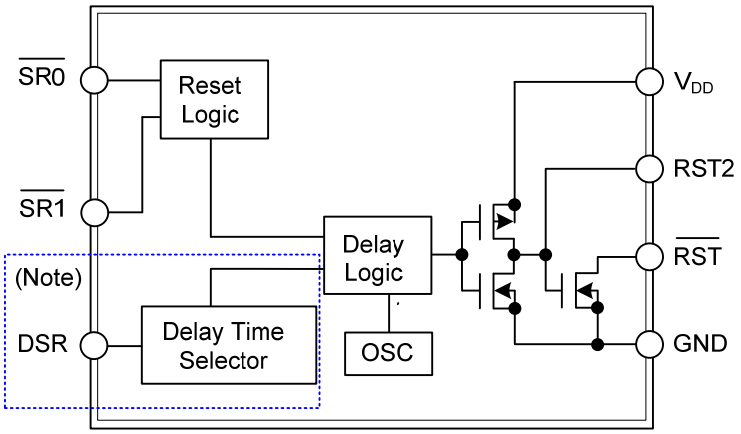
PIN NO.	PIN NAME	DESCRIPTION
1	NC	No Connection (UIC832A-x)
	RST2	CMOS Output Pin, Active-high (**UIC832B**)
2	GND	Ground Pin
3	$\overline{SR1}$	Input Pin2, Active-low (Note 1)
4	$\overline{RST}$	Nch Open Drain Output Pin, Active-low (Note 2)
5	DSR	Output Delay Time Selection Pin
	TEST2	Test Pin 2 (Note 3) (**UIC832X-Q, UIC832B-R, UIC832X-T**)
6	TEST	Test Pin (Note 3)
7	$\overline{SR0}$	Input Pin1, Active-low (Note 1)
8	V_{DD}	Power Supply Input Pin

Notes: 1. When only one active-low input pin is used, connect the unused one to GND.
2. The $\overline{RST}$ pin must be connected to GND or left floating if it is not used.
3. The TEST pin and the TEST2 pin must be connected to GND when they are used.

■ BLOCK DIAGRAM



UIC832A



UIC832B

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	6	V
Input Voltage (Input Pin1)	V_{SR0}	-0.3 ~ 6	V
Input Voltage (Input Pin2)	V_{SR1}	-0.3 ~ 6	V
Output Voltage (Reset Signal Output Pin1)	V_{RST}	-0.3 ~ 6	V
Output Voltage (Reset Signal Output Pin2)	V_{RST2}	-0.3 ~ 6.3	V
Output Current	I_{OUT}	20	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	-40 ~ +85	°C
Storage Temperature Range	T_{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

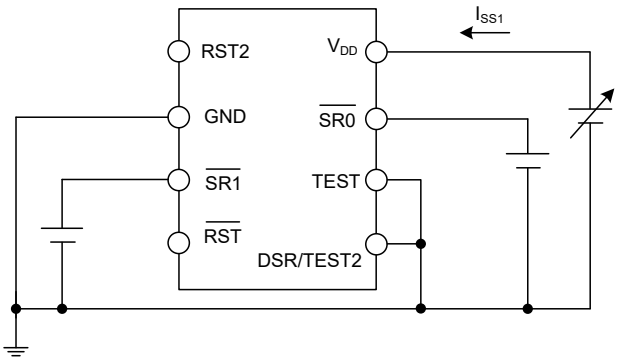
■ ELECTRICAL CHARACTERISTICS (Cont.) (T_A=25°C, unless otherwise specified)

UIC832X-Q, UIC832B-R, UIC832X-T

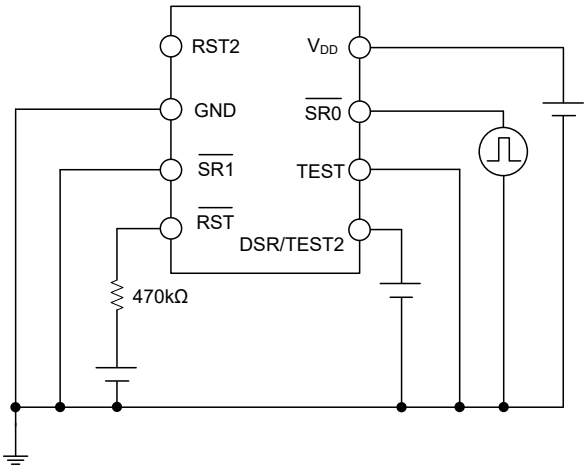
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}			1.65		5.5	V
Supply Current 1 (Note 1)	I_{SS1}	V_{DD}=5.5V (at standby)			0.55	1.35	μA
Supply Current 2 (Note 2)	I_{SS2}	V_{DD}=5.5V (at active before reset signal output)			1.2	6.5	μA
Supply Current 3 (Note 3)	I_{SS3}	V_{DD}=5.5V (at active after reset signal output)			0.15	1.7	μA
"L" Output Voltage	V_{OL}	$V_{DD} \geqq$ 4.5V, I_{OL}=8mA				0.3	V
		$V_{DD} \geqq$ 3.3V, I_{OL}=5mA				0.3	V
		$V_{DD} \geqq$ 1.65V, I_{OL}=3mA				0.5	V
"H" Output Voltage (Note 4)	V_{OH}	$V_{DD} \geqq$ 4.5V, I_{OL}=5mA		V_{DD} × 0.85			V
		$V_{DD} \geqq$ 3.3V, I_{OL}=2.5mA					
		$V_{DD} \geqq$ 1.65V, I_{OL}=0.8mA					
$\overline{SR0}$, $\overline{SR1}$ Input Leakage Current	I_{LEAKI}	V_{DD} = 5.5V				0.1	μA
Output Leakage Current	I_{LEAKO}	V_{DD} = 5.5V				0.1	μA
Output Delay Time (Note 5)	t_{Delay}	TEST1=TEST2=GND	UIC832X-Q	6.5	7.5	9.2	sec
			UIC832X-R	8.5	10	11.5	
			UIC 832X-T	2.6	3.0	3.6	
Output Release Time (Note 5)	t_{rec}	TEST1=TEST2=GND	UIC832X-Q	140	230	470	msec
			UIC832X-R	150	313	520	
			UIC 832X-T	130	180	280	
$\overline{SR0}$, $\overline{SR1}$ "L" Input Voltage	V_{IL}					0.3	V
$\overline{SR0}$, $\overline{SR1}$ "H" Input Voltage	V_{IH}			0.85			V

Notes: 1. Supply current when the device is active and waiting for the reset input.
2. Supply current when both active-low input pins are low and the timer operation is running.
3. Supply current after the completion of timer operation and the output of reset signal.
4. For the UTC **UIC832B** only (CMOS Output).
5. Refer to Output Delay Time and Output Release Time of **UIC832**.

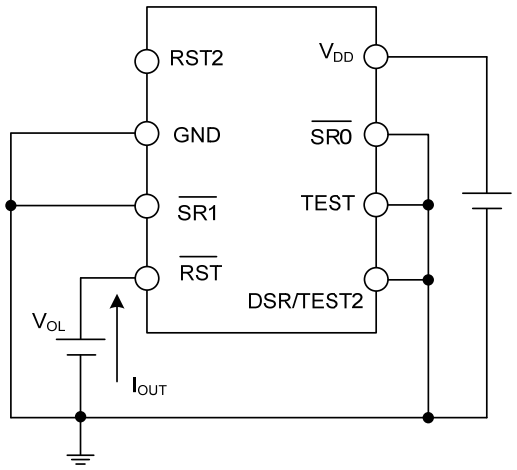
■ TEST CIRCUITS



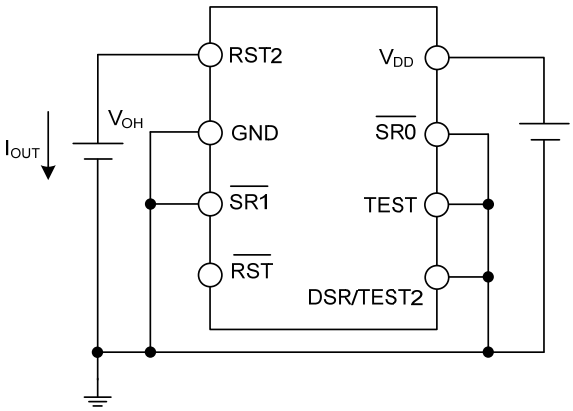
Supply Current Test Circuit



Output Delay Time Test Circuit

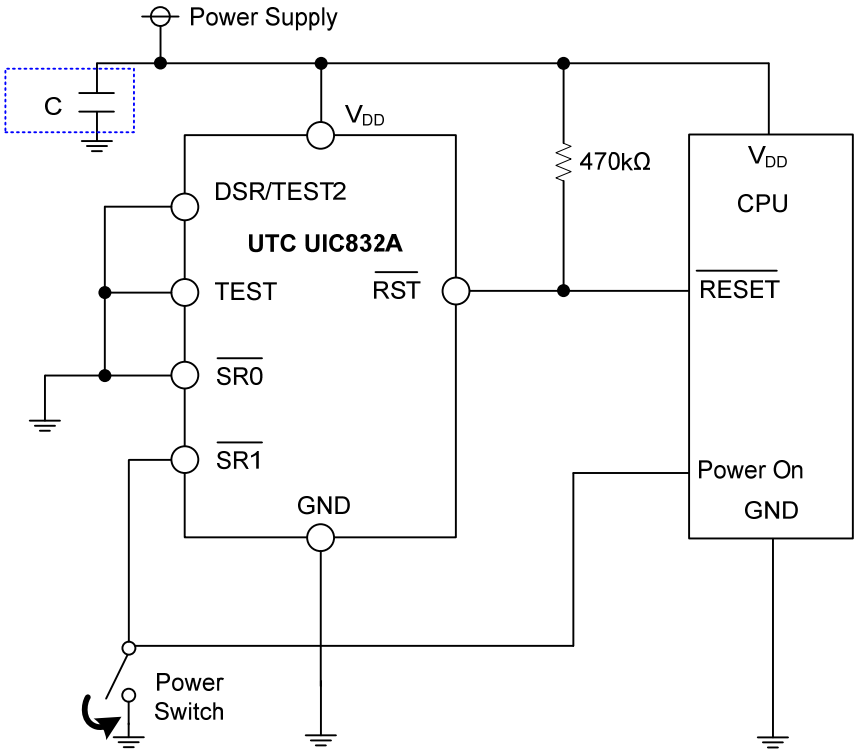


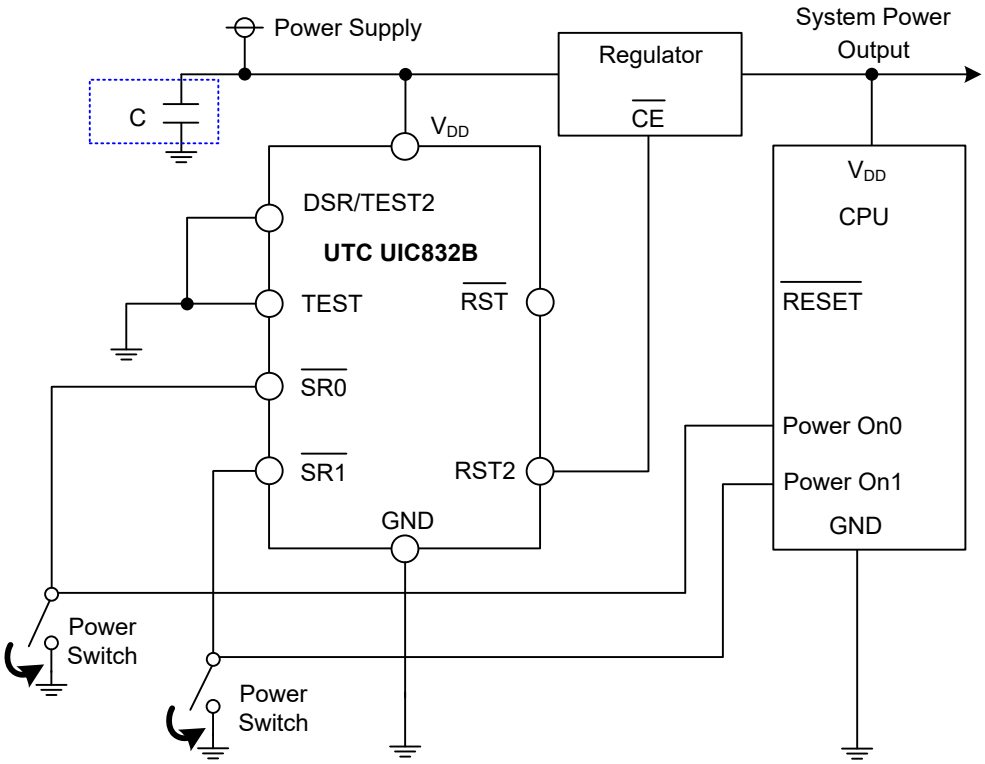
Nch Driver Output Voltage Test Circuit



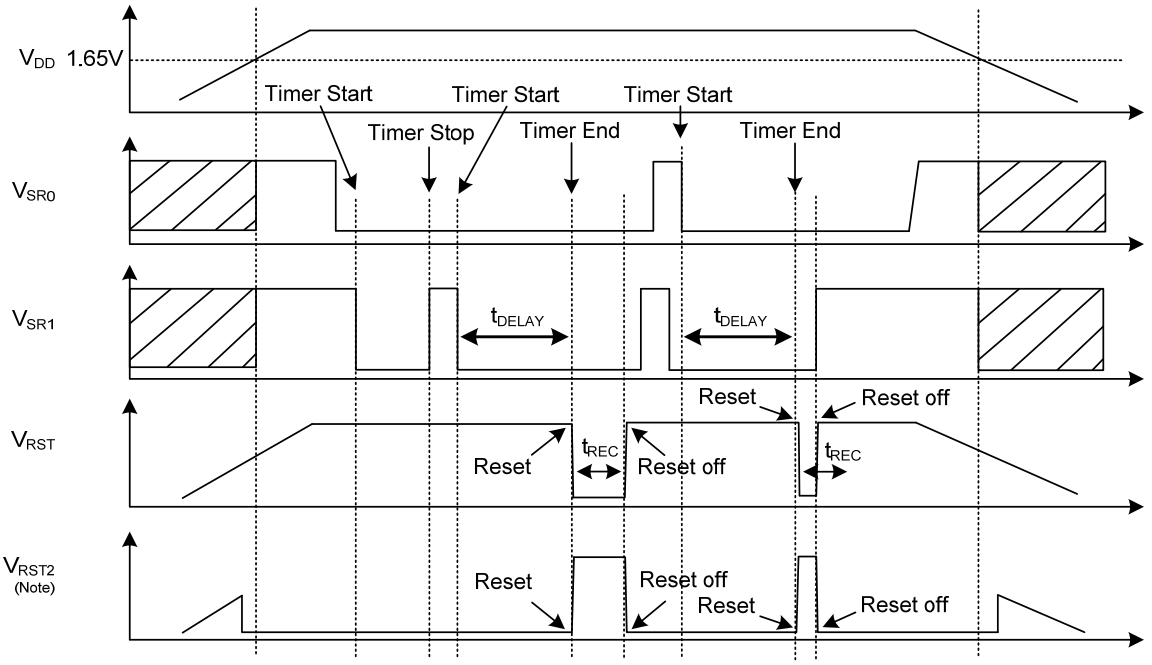
CMOS Driver Output Voltage Test Circuit
(For the **UIC832B** only.)

■ TYPICAL APPLICATION CIRCUIT





■ THEORY OF OPERATION



Note: For **UIC832B** only.

UIC832X-Q, UIC832B-R, UIC832X-T Timing Chart

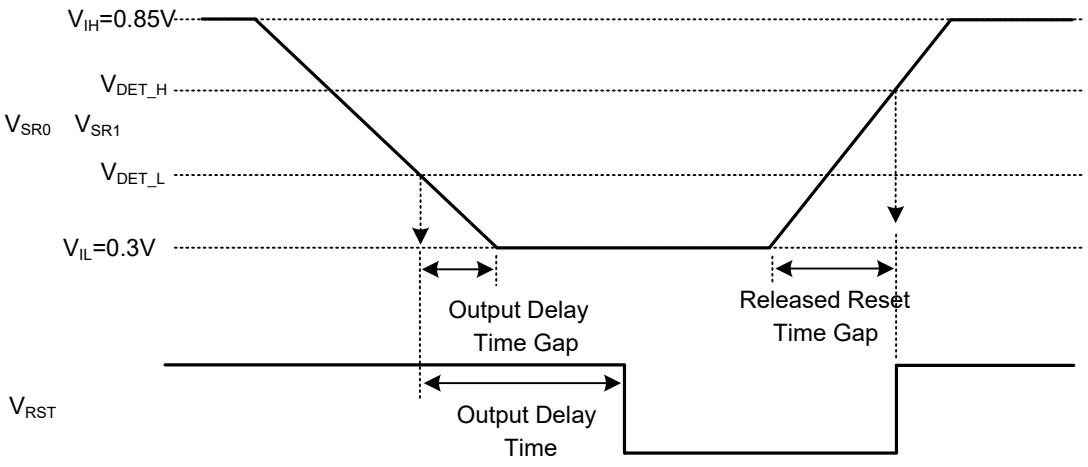
When both active-low input pins become the low voltage level, the timer operation starts. After the output delay time (tdelay), a reset signal will be sent out. If one of the active-low input pins becomes the high voltage level, the timer operation stops.

During tdelay, if one of the active-low input pins becomes the high voltage level, the timer operation stops. If both active-low input pins become the low voltage level again, a reset signal will be sent out after tdelay.

A reset signal will be released automatically after the reset delay time (trec), or it will be released if one of the active-low input pins becomes the high voltage level.

OUTPUT DELAY TIME GAP

The threshold voltages of the active-low input pins are between V_{IL} and V_{IH}. Therefore, if the rising or falling slew rate is very slow, the timer will start at the point of crossing the threshold voltage and may cause errors in the output delay time (tdelay) and the output release time (trec).



Relation between the Rising and Falling Slew Rate and the Time Gap

■ THEORY OF OPERATION (Cont.)

V_{DD} START-UP DURING LOW INPUT

When starting up V_{DD} at slow slew rate of 0.001V/μs or less while the active-low input pins are the low voltage level, the device may start the operation at lower than the minimum operating voltage, thus tdelay may exceed the guaranteed time.

■ TYPICAL CHARACTERISTICS