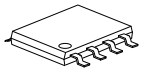
DUAL FET BUS SWITCH 2.5V/3.3V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH



TSSOP-8

■ DESCRIPTION

The **U74CB3Q3306** device is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (R_{ON}). The low and flat ON-state resistance allows for minimal propagation delay and supports switching input voltage beyond the supply on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the **U74CB3Q3306** device provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

This device is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to GND through a pull up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

■ FEATURES

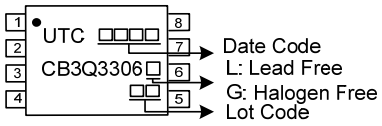
* Operation Voltage Range: 2.3 ~ 3.6V
* Low power consumption, 0.25mA Typ. I_{CC}
* High-bandwidth data path (up to 500 MHz)
* 5V tolerant I/Os with device powered up or powered down
* Low and flat ON-state resistance (R_{ON}) characteristics over operating range (Ron =4Ω typical)
* Supports input voltage beyond supply on data I/O ports
  0 to 5V switching with 3.3V V_{CC}
  0 to 3.3V switching with 2.5V V_{CC}
* Data I/Os support 0 to 5 V signaling levels (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, and 5V)
* Control inputs can be driven by TTL or 5V/3.3V CMOS outputs
* I_{OFF} supports partial-power-down mode operation

■ ORDERING INFORMATION

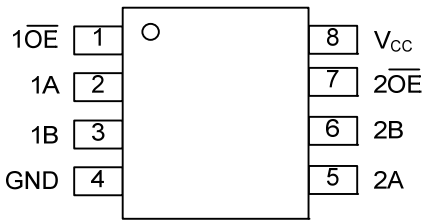
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CB3Q3306L-P08-R	U74CB3Q3306G-P08-R	TSSOP-8	Tape Reel

U74CB3Q3306G-P08-R (1)Packing Type (2)Package Type (3)Green Package	 (1) R: Tape Reel (2) P08: TSSOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION



■ PIN CONFIGURATION

PIN No	SYMBOL	TYPE	DESCRIPTION
1	1 $\overline{OE}$	I	Output Enable for Switch 1
2	1A	I/O	Channel 1A Port
3	1B	I/O	Channel 1B Port
4	GND	P	Ground
5	2A	I/O	Channel 2A Port
6	2B	I/O	Channel 2B Port
7	2 $\overline{OE}$	I	Output Enable for Switch 2
8	V_{CC}	P	Power Supply

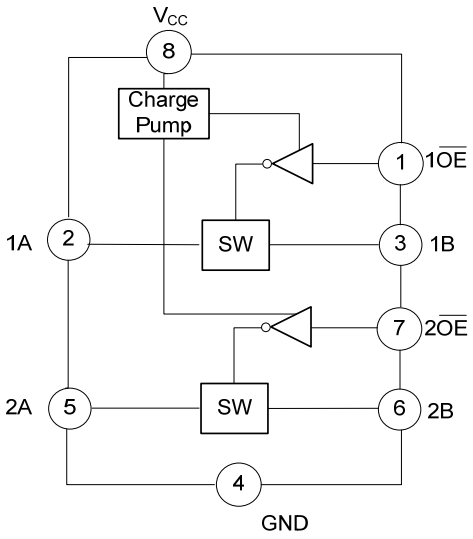
Note: I=Input, O=Output, I/O=Input and Output, P=Power.

■ FUNCTION TABLE (Each Bus Switch)

INPUT($\overline{OE}$)	INPUT(A)	FUNCTION
L	B	A Port = B Port
H	Z	Disconnect

Note: H: HIGH Voltage Level; L: LOW Voltage Level; Z=High-Impedance OFF-State.

■ LOGIC DIAGRAM (Positive Logic)



■ ABSOLUTE MAXIMUM RATINGS

over recommended operating free-air temperature range (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 4.6	V
Input Voltage	V_{IN}		-0.5 ~ 7	V
Switch I/O Voltage Range	$V_{I/O}$		-0.5 ~ 7	V
Input Clamp Current	I_{IK}	V_{IN} < 0V	-50	mA
I/O Port Clamp Current	$I_{I/OK}$	V_{OUT} < 0V	-50	mA
ON-State Switch Current	$I_{I/O}$		±64	mA
Continuous Current Through V_{CC} or GND			±100	mA
Junction Temperature	T_J		+150	°C
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
3. I_I and I_O are used to denote specific conditions for $I_{I/O}$.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	2.3		3.6	V
Switch I/O Voltage Range	$V_{I/O}$	0		5.5	V
Operating Temperature	T_A	-40		+125	°C

■ ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range (Unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage		V_{IH}	V_{CC}=2.3V~2.7V	1.7		5.5	V
			V_{CC}=2.7V~3.6V	2.0		5.5	V
Low-Lever Output Voltage		V_{IL}	V_{CC}=2.3V~2.7V	0		0.7	V
			V_{CC}=2.7V~3.6V	0		0.8	V
Clamp Diode Voltage		V_{IK}	V_{CC}=3.6V, I_I=-18mA			-1.8	V
Input Current	Control Inputs	I_{IN}	V_{CC}=3.6V, V_{OUT}=0~5.5V			±1	μA
Output OFF-state current (Note 3)		I_{OZ}	V_{CC}=3.6V, V_{OUT}=0~5.5V, V_{IN}=0, Switch OFF, V_{IN}=V_{CC} or GND			±1	μA
OFF-state output current		I_{OFF}	V_{CC}=0, V_{OUT}=0~5.5V, V_{IN}=0			1	μA
Quiescent Supply Current		I_{CC}	V_{CC}=3.6V, I_{IO}=0, Switch ON or OFF, V_{IN}=V_{CC} or GND		0.25	0.7	mA
Additional Quiescent Supply Current Per Input Pin	Control Inputs	ΔI_{CC} (Note 4)	V_{CC}=3.6V, One Input at 3V, Other Inputs at V_{CC} or GND			25	μA
	Per Control Input	I_{CCD} (Note 5)	V_{CC}=3.6V, A and B Ports Open, Control Input Switching at 50% duty cycle		0.03	0.1	mA/ MHz
Input Capacitance	Control Inputs	C_{IN}	V_{CC}=3.3V, V_{IN}=5.5V, 3.3V, 0		2.5	3.5	pF
OFF Output Capacitance		$C_{IO(OFF)}$	V_{CC}=3.3V, Switch OFF, V_{IN}=V_{CC} or GND, $V_{I/O}$=5.5V, 3.3V, 0		3.5	5.0	pF

■ ELECTRICAL CHARACTERISTICS (Cont.)

over recommended operating free-air temperature range (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ON Output Capacitance	$C_{IO(ON)}$	V_{CC}=3.3V, Switch ON, V_{IN}=V_{CC} or GND, $V_{I/O}$=5.5V, 3.3V, 0			8.0	10.5	pF
Static Drain-Source On-State Resistance (Note 6)	$R_{DS(ON)}$	V_{CC}=2.3V, TYP at V_{CC}=2.5V	V_{IN}=0, I_O=30mA		4.0	8.0	Ω
			V_{IN}=1.7V, I_O=-15mA		5.0	9.0	Ω
		V_{CC}=3.0V	V_{IN}=0, I_O=30mA		4.0	6.0	Ω
			V_{IN}=2.4V, I_O=-15mA		5.0	8.0	Ω

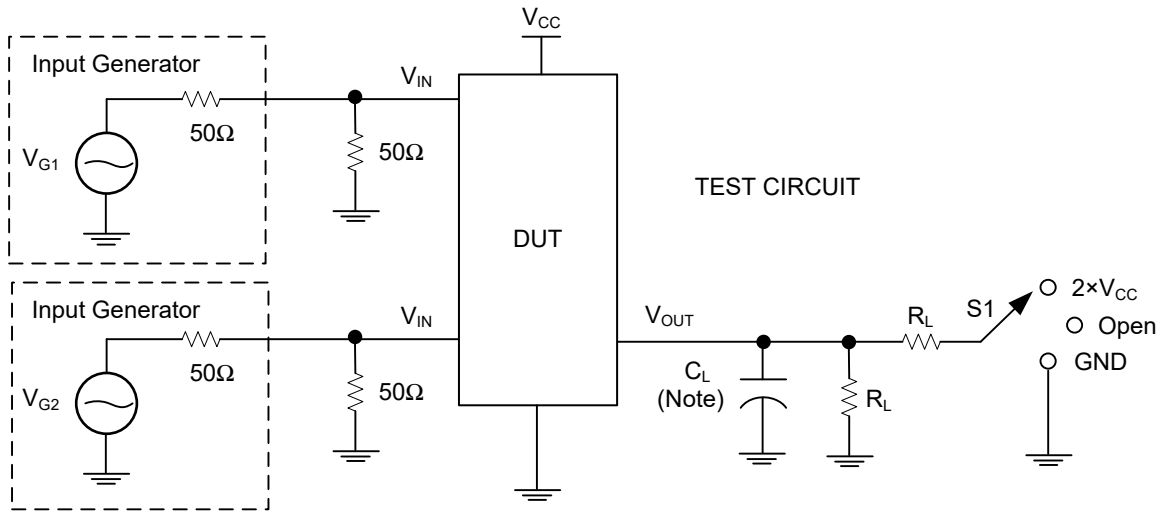
Notes: 1. V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
2. All typical values are at V_{CC}=3.3V (unless otherwise noted), T_A=25°C.
3. For I/O ports, the parameter IOZ includes the input leakage current.
4. This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
5. This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input.
6. Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

■ DYNAMIC CHARACTERISTICS (unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A=25°C			T_A=-40°C~+125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
From Input ($\overline{OE}$) to Output (A or B) (Note 1)	$f_{\overline{OE}}$	V_{CC}=2.5V±0.2V				10			10	MHz
		V_{CC}=3.3V±0.3V				20			20	MHz
Propagation Delay Time, From Input (A or B) to Output (B or A) (Note 2)	t_{PD} (t_{PLH}/t_{PHL})	C_L=15pF	V_{CC}=2.5V±0.2V			0.2			0.6	ns
		C_L=30pF	V_{CC}=3.3V±0.3V			0.2			0.6	ns
Enable Delay Time, From Input ($\overline{OE}$) to Output (A or B)	t_{en} (t_{PZL}/t_{PZH})	V_{CC}=2.5V±0.2V		1.0		11	1		12	ns
		V_{CC}=3.3V±0.3V		1.0		7.0	1		8.0	ns
Disable Delay Time, From Input ($\overline{OE}$) to Output (A or B)	t_{dis} (t_{PLZ}/t_{PHZ})	V_{CC}=2.5V±0.2V		1.0		5.5	1		6.5	ns
		V_{CC}=3.3V±0.3V		1.0		5.0	1		6.0	ns

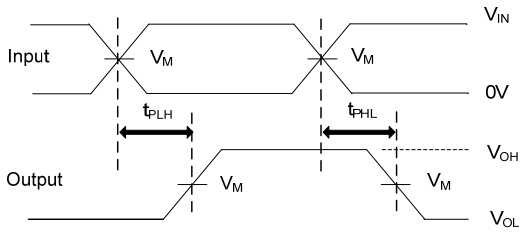
Notes: 1. Maximum switching frequency for control input (V_O > V_{CC}, V_I = 5V, R_L ≧ 1MΩ, C_L = 0).
2. The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

■ TEST CIRCUIT AND WAVEFORMS

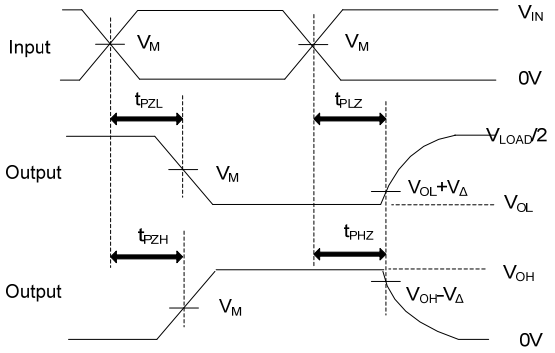


Note: C_L includes probe and jig capacitance.

TEST	V_{CC}	S1	R_L	V_{IN}	C_L	V_Δ
t_{PD} (t_{PLH}/t_{PHL})	2.5V±0.2V	Open	500Ω	V_{CC} or GND	30pF	
	3.3V±0.3V	Open	500Ω	V_{CC} or GND	50pF	
t_{en} (t_{PZL}/t_{PZH})	2.5V±0.2V	2×V_{CC}	500Ω	GND	30pF	0.15V
	3.3V±0.3V	2×V_{CC}	500Ω	GND	50pF	0.3V
t_{dis} (t_{PLZ}/t_{PHZ})	2.5V±0.2V	GND	500Ω	V_{CC}	30pF	0.15V
	3.3V±0.3V	GND	500Ω	V_{CC}	50pF	0.3V



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and test-fixture capacitance
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O= 50Ω, t_r < 2.5ns, t_f < 2.5ns.