

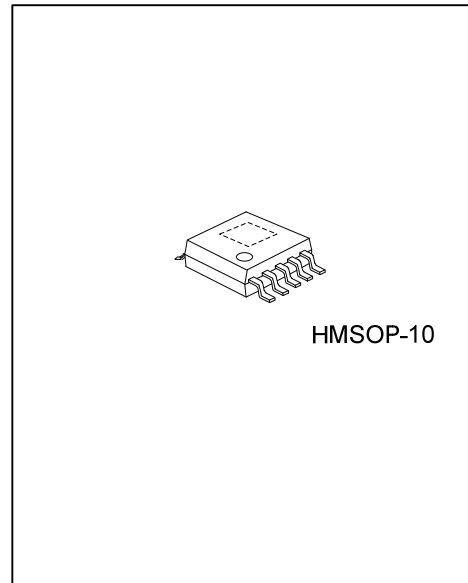


## ALDR8905

Preliminary

CMOS IC

### CAPLESS 2 V<sub>RMS</sub> TO 3 V<sub>RMS</sub> LINE DRIVER WITH ADJUSTABLE GAIN



#### DESCRIPTION

The UTC **ALDR8905** is a 2V<sub>RMS</sub> to 3V<sub>RMS</sub> pop/click-free stereo line driver designed to allow the removal of the output DC-blocking capacitors for reduced component count and cost. The device is ideal for single supply electronics where size and cost are critical design parameters.

The UTC **ALDR8905** is capable of driving 2V<sub>RMS</sub> into a 2.5kΩ load with 3.3V supply voltage. The device has single input and uses external gain setting resistors that supports a gain range of ±1V/V to ±10V/V. The **ALDR8905** has build-in shutdown control for pop/click-free on/off control.

#### FEATURES

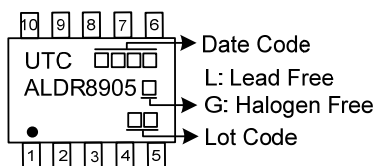
- \* Integrated Charge pump generates negative supply rail
- \* Provides flat frequency response from DC to 20kHz
- \* Pop-Free under-voltage protection
- \* Low noise and THD  
Typical THD+N = 0.001% (f = 1kHz)
- \* 2V<sub>RMS</sub> output voltage into 2.5kΩ load with 3.3V supply voltage
- \* 3V<sub>RMS</sub> output voltage into 2.5kΩ load with 5V supply voltage

#### ORDERING INFORMATION

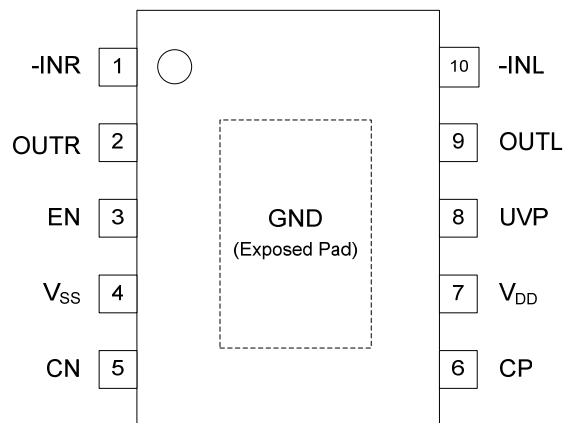
Ordering Number		Package	Packing
Lead Free	Halogen Free		
ALDR8905L-HM2-R	ALDR8905G-HM2-R	HMSOP-10	Tape Reel

<p>ALDR8905G-HM2-R</p> <ul style="list-style-type: none"> <li>(1) Packing Type</li> <li>(2) Package Type</li> <li>(3) Green Package</li> </ul>	<ul style="list-style-type: none"> <li>(1) R: Tape Reel</li> <li>(2) HM2: HMSOP-10</li> <li>(3) G: Halogen Free and Lead Free, L: Lead Free</li> </ul>
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#### MARKING



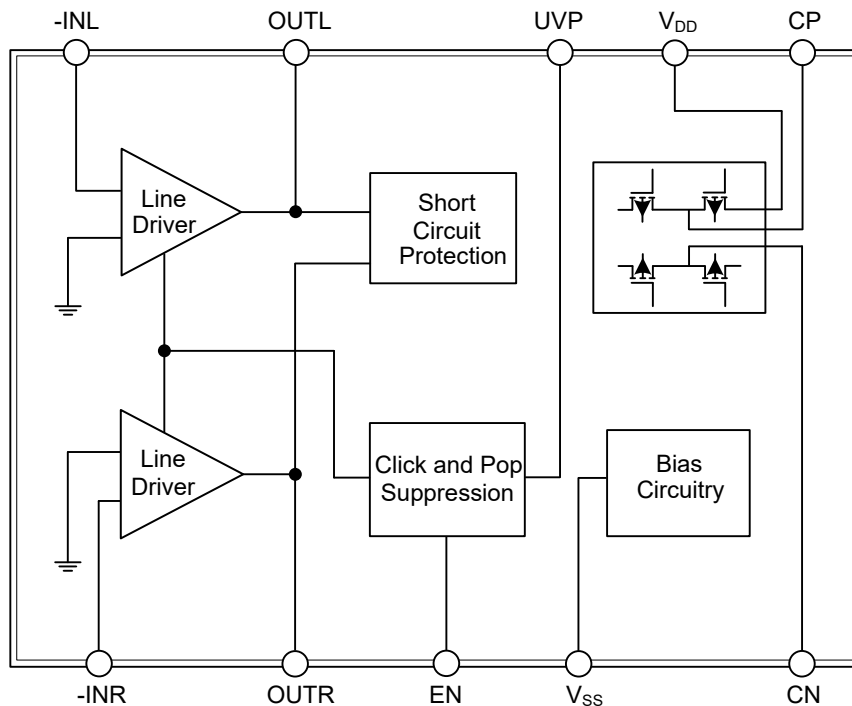
### ■ PIN CONFIGURATION



### ■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	-INR	Right Channel OPAMP Negative Input
2	OTR	Right Channel OPAMP Output
3	EN	Enable Input. Active high
4	V <sub>SS</sub>	Negative Supply Voltage
5	CN	Charge Pump Flying Capacitor Negative Terminal
6	CP	Charge Pump Flying Capacitor Positive Terminal
7	V <sub>DD</sub>	Positive Supply Voltage
8	UVP	Under-Voltage Protection Input
9	OUTL	Left Channel OPAMP Output
10	-INL	Left Channel OPAMP Negative Input
Exposed Pad	GND	Exposed Pad. Can only be connected to GND

### ■ BLOCK DIAGRAM



### ■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{DD}$	-0.3 ~ 6	V
Input Voltage	$V_{IN}$	$V_{SS} - 0.3 \sim V_{DD} + 0.3$	V
Minimum Load Impedance	$R_L$	600	$\Omega$
EN to GND		-0.3 ~ $V_{DD} + 0.3$	V
Lead Temperature (Soldering, 10s)		+260	$^{\circ}\text{C}$
Junction Temperature	$T_J$	+150	$^{\circ}\text{C}$
Storage Temperature	$T_{STG}$	-65 ~ +150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

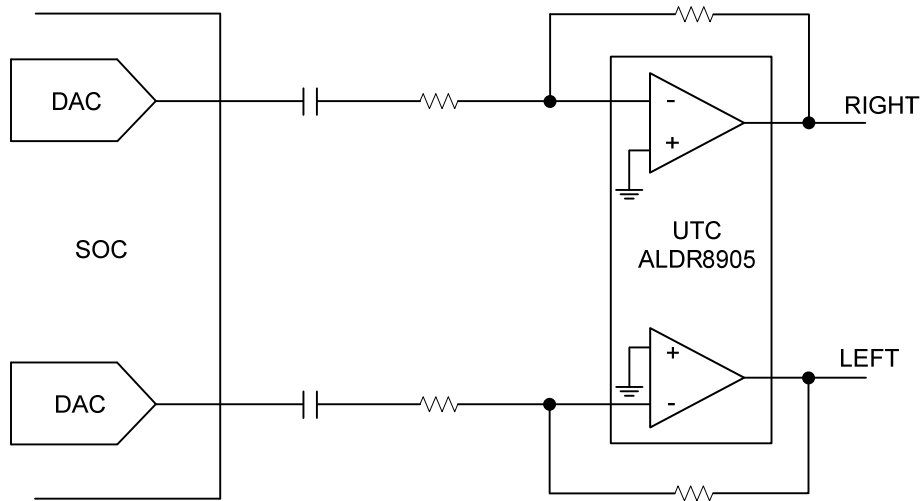
### ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{DD}$	3 ~ 5.5	V
Operating Temperature	$T_A$	-40 ~ +85	$^{\circ}\text{C}$

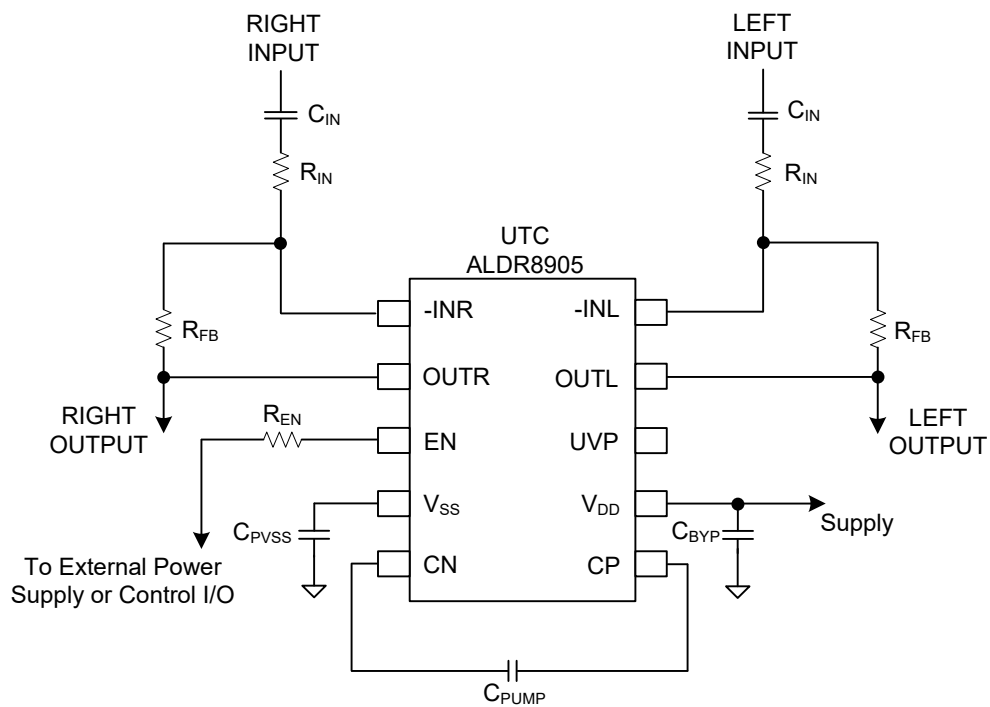
### ■ ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ELECTRICAL CHARACTERISTICS</b>						
DC Supply Voltage	$V_{DD}$		3		5.5	V
Output Offset Voltage	$ V_{OS} $	$V_{DD}=3\sim 5\text{V}$	-5.5		5.5	mV
Power Supply Rejection Ratio	PSRR	$V_{DD}=3\sim 5\text{V}$		97		dB
High-Level Output Voltage	$V_{OH}$	$V_{DD}=3.3\text{V}$ , $R_L=2.5\text{k}\Omega$	3.1			V
Low-Level Output Voltage	$V_{OL}$	$V_{DD}=3.3\text{V}$ , $R_L=2.5\text{k}\Omega$			-3.05	V
High-Level Input Current (EN)	$ I_{IH} $	$V_{DD}=5\text{V}$ , $V_I=V_{DD}$			1	$\mu\text{A}$
Low-Level Input Current (EN)	$ I_{IL} $	$V_{DD}=5\text{V}$ , $V_I=0\text{V}$			1	$\mu\text{A}$
Supply Current	$I_{DD}$	$V_{DD}=3.3\text{V}$ , No load, EN= $V_{DD}$		7	14.5	mA
		$V_{DD}=5\text{V}$ , No load, EN= $V_{DD}$		9.5	15.5	mA
		Shutdown mode, $V_{DD}=3\text{V}$ to $5\text{V}$		0.15	0.25	mA
<b>OPERATING CHARACTERISTICS</b> ( $V_{DD}=3.3\text{V}$ , $R_L=2.5\text{k}\Omega$ , $C_{PUMP}=C_{PVSS}=1\mu\text{F}$ , $C_{IN}=10\mu\text{F}$ , $R_{IN}=10\text{k}\Omega$ , $R_{FB}=20\text{k}\Omega$ .)						
Output Voltage (Outputs In Phase)	$V_O$	THD=1%, $V_{DD}=3.3\text{V}$ , $f=1\text{kHz}$	2.05			$V_{RMS}$
		THD=1%, $V_{DD}=5\text{V}$ , $f=1\text{kHz}$	3.05			$V_{RMS}$
Total Harmonic Distortion Plus Noise	THD+N	$V_O=2V_{RMS}$ , $f=1\text{kHz}$		0.001		%
Crosstalk	$X_{TALK}$	$V_O=2V_{RMS}$ , $f=1\text{kHz}$		-103		dB
Output Current Limit	$I_O$	$V_{DD}=3.3\text{V}$		20		mA
Input Resistor Range	$R_{IN}$			10		$\text{k}\Omega$
Feedback Resistor Range	$R_{FB}$			20		$\text{k}\Omega$
Slew Rate	SR			10		$\text{V}/\mu\text{s}$
Maximum Capacitive Load	$C_L$			220		pF
Noise Output Voltage	$V_N$	A-weighted, $\text{BW}=20\text{kHz}$		5.4		$\mu\text{V}_{RMS}$
Signal to Noise Ratio	SNR	A-weighted, $V_O=2V_{RMS}$ , $\text{BW}=20\text{kHz}$		108		dB
Unity Gain Bandwidth	$G_{BW}$			8		MHz
Open-Loop Voltage Gain	$A_{VO}$			100		dB
Charge Pump Frequency	$F_{CP}$		300		600	kHz
External Under-Voltage Detection	$V_{UVP}$		1	1.15	1.3	V
External Under-Voltage Detection Hysteresis Current	$I_{Hys}$			4.8		$\mu\text{A}$
<b>EN PIN</b>						
Input High Voltage	$V_{INH}$	EN	1.2			V
Input Low Voltage	$V_{INL}$	EN			0.3	V

■ TYPICAL OPERATION CIRCUIT



■ TYPICAL APPLICATION CIRCUIT



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