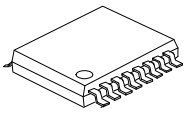
4-CHANNEL I²C AND SMBUS SWITCH WITH RESET FUNCTION



TSSOP-16

DESCRIPTION

The UTC **UCA9546** is a quad bidirectional translating switch controlled via the I²C bus. The SCL/SDA upstream pair fans out to four downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register.

An active-low reset ($\overline{\text{RESET}}$) input allows the UTC **UCA9546** to recover from a situation in which one of the downstream I2C buses is stuck in a low state. Pulling $\overline{\text{RESET}}$ low resets the I2C state machine and causes all the channels to be deselected, as does the internal power-on reset function.

The pass gates of the switches are constructed such that the V_{CC} pin can be used to limit the maximum high voltage which is passed by the **UCA9546**. This allows the use of different bus voltages on each pair, so that 1.8V or 2.5V or 3.3V parts can communicate with 5V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5.5V tolerant.

■ FEATURES

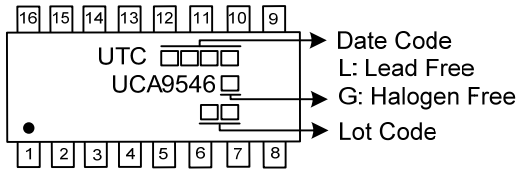
* 1-of-4 Bidirectional Translating Switches
* I²C Bus and SMBus Compatible
* Active-Low Reset Input
* 3 Address Pins, Allowing up to Eight Devices on the I²C Bus
* Channel Selection Via I²C Bus
* Power Up With All Switch Channels Deselected
* Low R_{ON} Switches
* Allows Voltage-Level Translation Between 1.8V, 2.5V, 3.3V, and 5V Buses
* No Glitch on Power Up
* Supports Hot Insertion
* Low Standby Current
* Operating Power-Supply Voltage Range of 2.3 V to 5.5 V
* 5.5V Tolerant Inputs
* 0 to 400kHz Clock Frequency

■ ORDERING INFORMATION

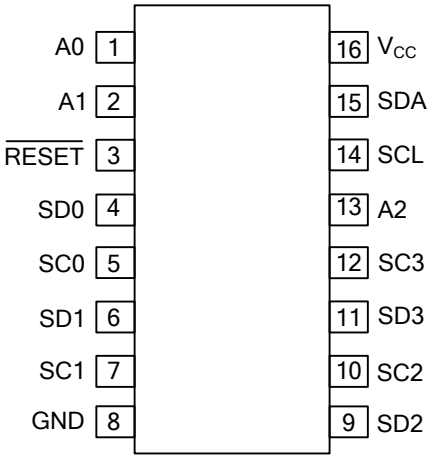
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCA9546L-P16-R	UCA9546G-P16-R	TSSOP-16	Tape Reel

UCA9546G-P16-R (1) Packing Type (2) Package Type (3) Green Package	 (1) R: Tape Reel (2) P16: TSSOP-16 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



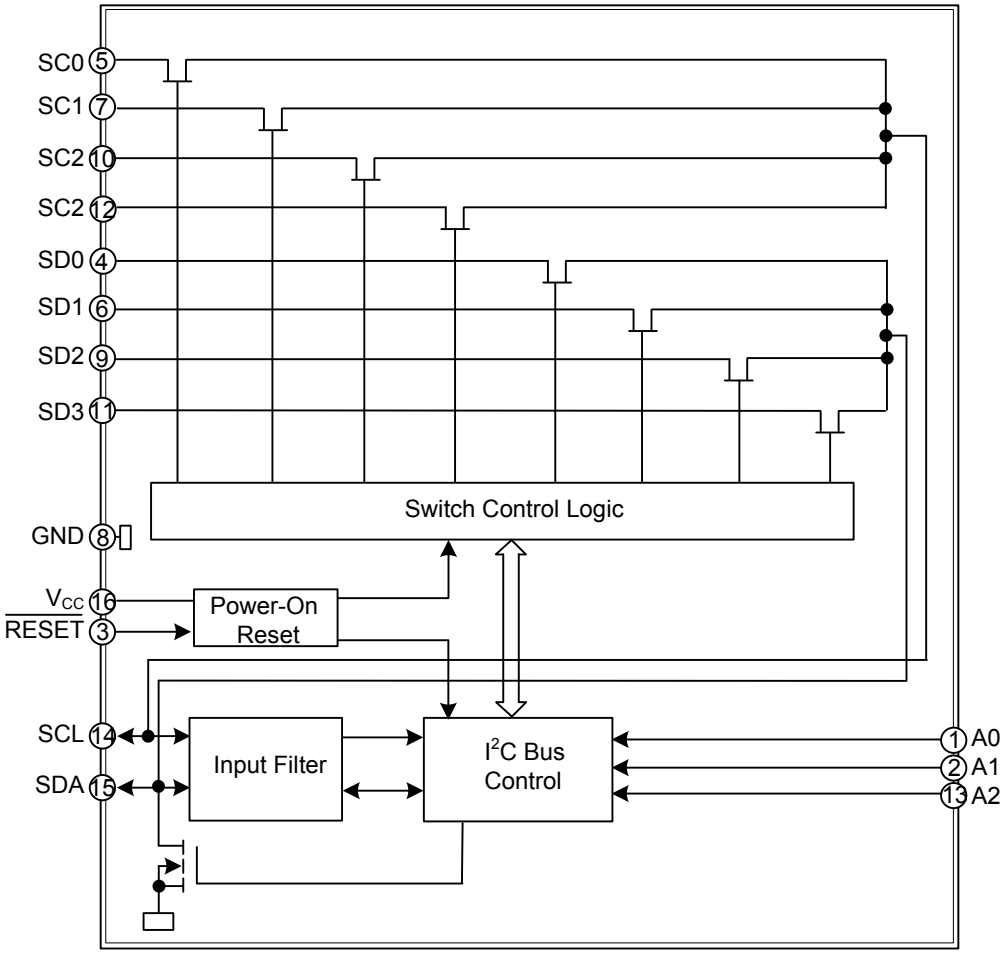
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	A0	Address input 0. Connect directly to V_{CC} or ground
2	A1	Address input 1. Connect directly to V_{CC} or ground
3	$\overline{\text{RESET}}$	Active low reset input. Connect to V_{CC} through a pullup resistor, if not used.
4	SD0	Serial data 0. Connect to V_{CC} through a pullup resistor
5	SC0	Serial clock 0. Connect to V_{CC} through a pullup resistor
6	SD1	Serial data 1. Connect to V_{CC} through a pullup resistor
7	SC1	Serial clock 1. Connect to V_{CC} through a pullup resistor
8	GND	Ground
9	SD2	Serial data 2. Connect to V_{CC} through a pullup resistor
10	SC2	Serial clock 2. Connect to V_{CC} through a pullup resistor
11	SD3	Serial data 3. Connect to V_{CC} through a pullup resistor
12	SC3	Serial clock 3. Connect to V_{CC} through a pullup resistor
13	A2	Address input 2. Connect directly to V_{CC} or ground
14	SCL	Serial clock line. Connect to V_{CC} through a pullup resistor
15	SDA	Serial data line. Connect to V_{CC} through a pullup resistor
16	V_{CC}	Supply power

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
Input Voltage Range (Note 2)	V_I	-0.5 ~ 7	V
Input Current	I_I	±20	mA
Output Current	I_O	±25	mA
Continuous Current Through V_{CC}		±100	mA
Continuous Current Through GND		±100	mA
Total Power Dissipation	P_{TOT}	400	mW
Operating Free-Air Temperature Range	T_A	-40 ~ +85	°C
Storage Temperature	T_{STG}	-65~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	110	°C/W

■ RECOMMENDED OPERATING CONDITIONS (NOTE)

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CC}	2.3		5.5	V
High-Level Input Voltage	SCL, SDA	V_{IH}	0.7 × V_{CC}		6	V
	A2-A0, $\overline{\text{RESET}}$		0.7 × V_{CC}		V_{CC}+0.5	V
Low-Level Input Voltage	SCL, SDA	V_{IL}	-0.5		0.3×V_{CC}	V
	A2-A0, $\overline{\text{RESET}}$		-0.5		0.3×V_{CC}	V
Operating Free-Air Temperature		T_A	-40		+85	°C

Note: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
Power-On Reset Voltage (Note 2)		V_{POR}	No Load, V_I=V_{CC} or GND, V_{CC}=V_{POR}			1.6		V
Switch Output Voltage		V_{pass}	V_{CC}=5V	V_{SWin}=V_{CC}, I_{SWout} =-100μA		3.6		V
			V_{CC}=4.5V~ 5.5V		2.6		4.5	V
			V_{CC}=3.3V			1.9		V
			V_{CC}=3V~3.6V		1.6		2.8	V
			V_{CC}=2.5V			1.5		V
			V_{CC}=2.3V~2.7V		1.1		2	V
Low-Level Output Current	SCL, SDA	I_{OL}	V_{CC}=2.3V~5.5V	V_{OL}=0.4V	3	7		mA
				V_{OL}=0.6V	6	10		mA
Input Leakage	SCL, SDA	I_I	V_{CC}=2.3V~ 5.5V	V_I=V_{CC} or GND			±1	μA
	SC3-SC0, SD3-SD0						±1	μA
	A2-A0						±1	μA
	$\overline{\text{RESET}}$						±1	μA
Operating Mode	f_{SCL}=100kHz	I_{CC}	V_{CC}=5.5V	V_I=V_{CC} or GND, I_O=0		55		μA
			V_{CC}=3.6V			55		μA
			V_{CC}=2.7V			55		μA
Standby Mode	Low Inputs		V_{CC}=5.5V	V_I=GND, I_O=0		0.2	2	μA
			V_{CC}=3.6V			0.1	1.3	μA
			V_{CC}=2.7V			0.1	1.1	μA
	High Inputs		V_{CC}=5.5V	V_I=V_{CC}, I_O=0		0.2	2	μA
			V_{CC}=3.6V			0.1	1.3	μA
			V_{CC}=2.7V			0.1	1.1	μA
Supply-Current Change	SCL, SDA	ΔI_{CC}	SCL or SDA Input at 0.6V, Other Inputs at V_{CC} or GND			20	50	μA
			SCL or SDA input at V_{CC}-0.6V, Other Inputs at V_{CC} or GND	V_{CC}=2.3V~ 5.5V		20	50	μA
Input Capacitance	A2-A0	C_I	V_{CC}=2.3V~5.5V	V_I=V_{CC} or GND		4.5		pF
	$\overline{\text{RESET}}$					4.5		pF
Output Capacitance	SCL, SDA	$C_{IO(OFF)}$ (Note 3)	V_{CC}=2.3V~5.5V	V_I=V_{CC} or GND, Switch OFF		15		pF
	SC3-SC0, SD3-SD0		V_{CC}=2.3V~5.5V			6		pF
Switch On-State Resistance		R_{ON}	V_{CC}=4.5V~5.5V	V_O=0.4V, I_O=15mA	4	12	20	Ω
			V_{CC}=3V~3.6V		5	15	25	Ω
			V_{CC}=2.3V~ 2.7V ,	V_O=0.4V, I_O=10mA	7	21	50	Ω

Notes: 1. All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}), T_A = 25°C.

2. The power-on reset circuit resets the I^2C bus logic with V_{CC} < V_{POR}. V_{CC} must be lowered to 0.2 V to reset the device.

3. $C_{io(ON)}$ depends on internal capacitance and external capacitance added to the SCn lines when channels(s) are ON

■ I²C INTERFACE TIMING REQUIREMENTS

(T_A=25°C, unless otherwise specified) (see Figure 1)

PARAMETER		SYMBOL	STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
I²C Clock Frequency		f_{scl}	0	100	0	400	kHz
I²C Clock High Time		t_{sch}	4		0.6		μs
I²C Clock Low Time		t_{scl}	4.7		1.3		μs
I²C Spike Time		t_{sp}		50		50	ns
I²C Serial-Data Setup Time		t_{sds}	250		100		ns
I²C Serial-Data Hold Time		t_{sdh}	0 (Note 1)		0 (Note 1)		μs
I²C Input Rise Time		t_{icr}		1000		300	ns
I²C Input Fall Time		t_{icf}		300		300	ns
I²C Output Fall Time	10-pF to 400-pF Bus	t_{ocf}		300		300	ns
I²C Bus Free Time between Stop and Start		t_{buf}	4.7		1.3		μs
I²C Start or Repeated Start Condition Setup		t_{sts}	4.7		0.6		μs
I²C Start or Repeated Start Condition Hold		t_{sth}	4		0.6		μs
I²C Stop Condition Setup		t_{sps}	4		0.6		μs
Valid-Data Time (High to Low) (Note 2)	SCL Low to SDA Output Low Valid	$t_{vdL(Data)}$		1		1	μs
Valid-Data Time (Low to High) (Note 2)	SCL Low to SDA Output High Valid	$t_{vdH(Data)}$		0.6		0.6	μs
Valid-Data Time of ACK Condition	ACK Signal from SCL Low to SDA Output Low	$t_{vd(ack)}$		1		1	μs

Notes: 1. A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to as the V_{IH} min of the SCL signal), in order to bridge the undefined region of the falling edge of SCL.
2. Data taken using a 1-kΩ pull-up resistor and 50-pF load (see Figure 1).

■ SWITCHING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

(C_L ≤ 100pF, unless otherwise specified) (see Figure 1).

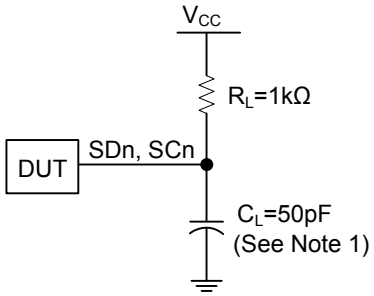
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From Input (SDA or SCL) to Output (SDn or SCn)	t_{PD}	V_{CC}=2.3V, C_L=50pF		12	25	ns
		V_{CC}=5.5V, C_L=50pF		6	11	ns

■ INTERRUPT AND RESET TIMING REQUIREMENTS (T_A=25°C, unless otherwise specified)

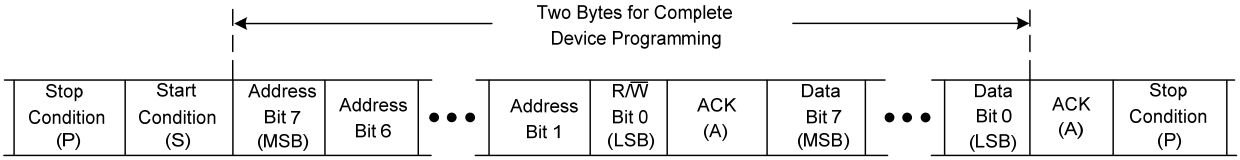
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pulse Duration, $\overline{\text{RESET}}$ Low	t_{WL}		6			ns
$\overline{\text{RESET}}$ Time (SDA Clear)	t_{rst} (Note 1)				500	ns
Recovery Time from $\overline{\text{RESET}}$ to Start	$t_{REC(STA)}$		0			ns

Note: t_{rst} is the propagation delay measured from the time the $\overline{\text{RESET}}$ pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of t_{WL}.

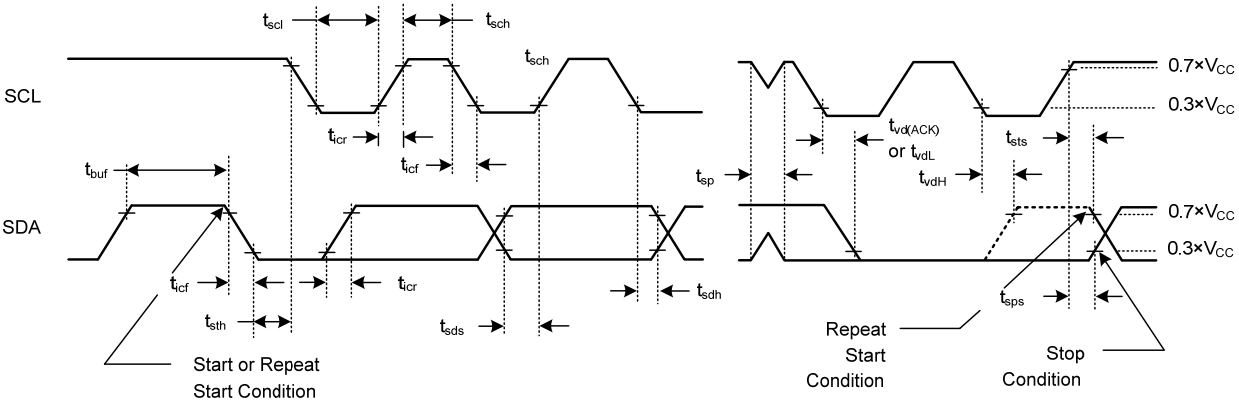
■ PARAMETER MEASUREMENT INFORMATION



I^2C Port Load Configuration



BYTE	DESCRIPTION
1	I^2C address + R/$\overline{W}$
2	Control register data



Voltage Waveforms

Notes 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O=50Ω, t_r/t_f=30ns.

3. The outputs are measured one at a time, with one transition per measurement.

Figure 1. I^2C Interface Load Circuit, Byte Descriptions, and Voltage Waveforms

■ PARAMETER MEASUREMENT INFORMATION

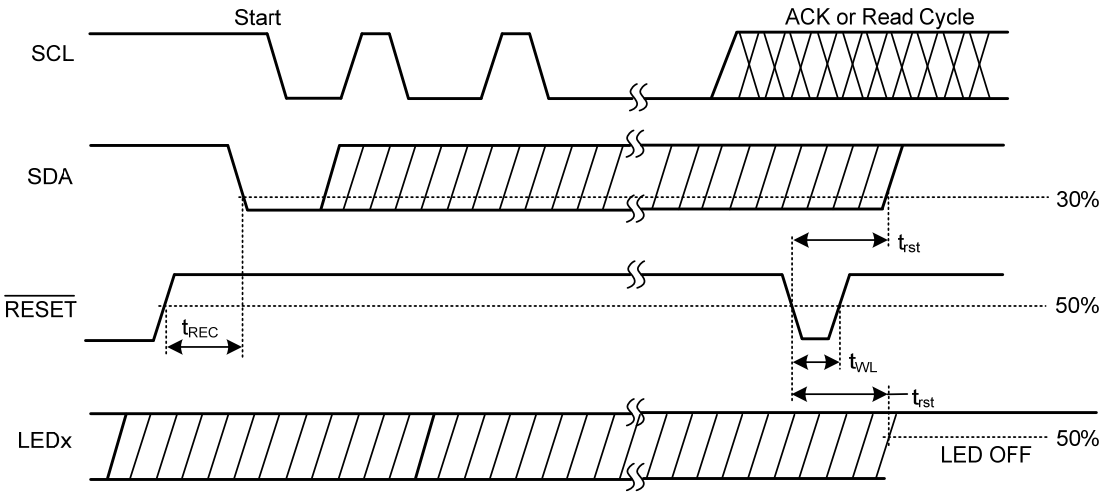


Figure 2. Reset Timing

■ TYPICAL APPLICATION CIRCUIT

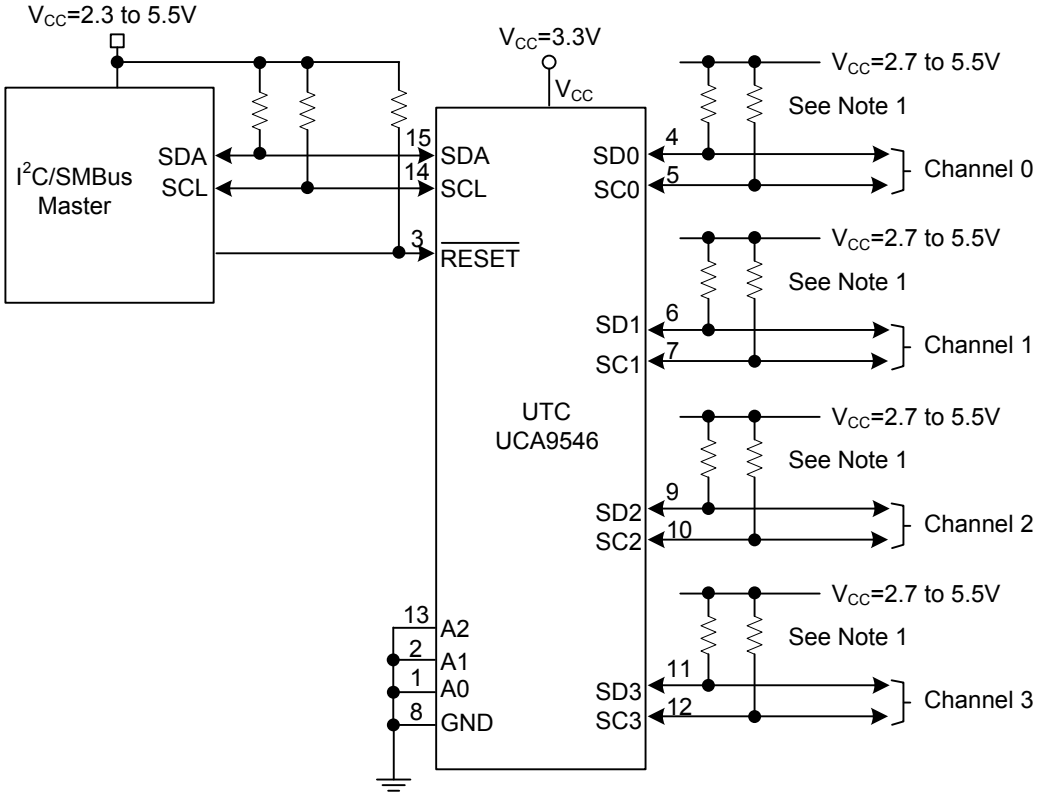


Figure 3. Typical Application