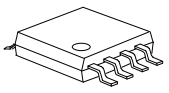
LEVEL TRANSLATING I²C-BUS REPEATER



MSOP-8

■ DESCRIPTION

The UTC **UCA9517** is a CMOS integrated circuit that provides level shifting between low voltage (down to 0.9 V) and higher voltage (2.7V to 5.5V) I^2C-bus or SMBus applications. While retaining all the operating modes and features of the I^2C-bus system during the level shifts, it also permits extension of the I^2C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines using the UTC **UCA9517** enables the system designer to isolate two halves of a bus for both voltage and capacitance. The SDA and SCL pins are over voltage tolerant and are high-impedance when the UTC **UCA9517** is unpowered.

The UTC **UCA9517** drivers are not enabled unless V_{CCA} is above 0.8V and V_{CC} is above 2.5V. The EN pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle.

The output pull-down on the B-side internal buffer LOW is set for approximately 0.5V, while the input threshold of the internal buffer is set about 80mV lower (0.42V). When the B-side I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the A-side drives a hard LOW and the input level is set at $0.25\times V_{CCA}$ to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.9V.

■ FEATURES

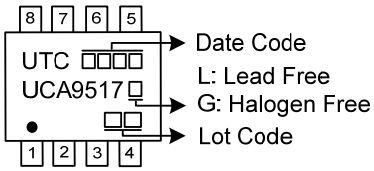
* Voltage level translation from 0.9V to 5.5V and from 2.7V to 5.5V
* I^2C-bus and SMBus compatible
* Active HIGH repeater enable input
* Open-drain input/outputs
* Lock-up free operation
* Supports arbitration and clock stretching across the repeater
* Accommodates Standard mode and Fast mode I^2C-bus devices and multiple masters
* Powered-off high-impedance I^2C-bus pins
* A-side operating supply voltage range of 0.9V to 5.5V
* B-side operating supply voltage range of 2.7V to 5.5V
* 5 V tolerant I^2C-bus and enable pins
* 0 Hz to 400 kHz clock frequency (the maximum system operating frequency may beless than 400 kHz because of the delays added by the repeater).

■ ORDERING INFORMATION

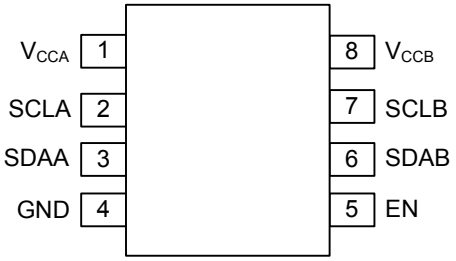
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCA9517L-SM1-R	UCA9517G-SM1-R	MSOP-8	Tape Reel

UCA9517G-SM1-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) SM1: MSOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



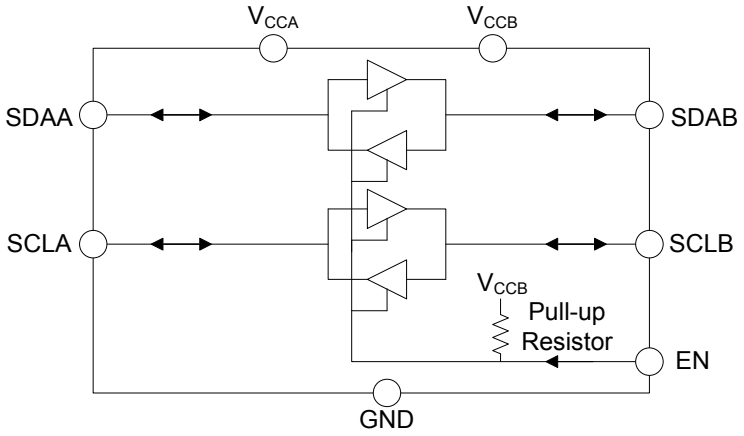
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{CCA}	A-side supply Voltage (0.9V to 5.5V)
2	SCLA	serial clock A-side bus
3	SDAA	serial data A-side bus
4	GND	supply ground (0V)
5	EN	active HIGH repeater enable input
6	SDAB	serial data B-side bus
7	SCLB	serial clock B-side bus
8	V_{CCB}	B-side supply Voltage (2.7V to 5.5V)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage, A-Side Bus	V_{CCA}	Adjustable	-0.5 ~ 7.0	V
Supply Voltage, B-Side Bus	V_{CCB}	2.7V to 5.5V	-0.5 ~ 7.0	V
Voltage On I^2C-bus B-side, or Enable (EN)	V_{BUS}		-0.5 ~ 7.0	V
DC Current	I_I	Any Pin	50	mA
Total Power Dissipation	P_D		100	mW
Junction Temperature	T_J		+125	°C
Storage Temperature	T_{STG}		-55 ~ +125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Ambient Temperature	T_A	Operating in Free Air	-40		+85	°C

■ ELECTRICAL CHARACTERISTICS

(V_{CC}=2.7V to 5.5V, GND=0V, T_A= −40 °C to +85 °C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLIES						
Supply Voltage, B-Side Bus	V_{CCB}		2.7		5.5	V
Supply Voltage, A-Side Bus	V_{CCA}	(Note 1)	0.9		5.5	V
Supply Current on Pin V_{CCA}	$I_{CC(VCCA)}$				1	mA
HIGH-State Supply Current	I_{CCH}	Both Channels HIGH V_{CC}=5.5V, SDAn=SCLn=V_{CC}		1.5	5	mA
LOW-State Supply Current	I_{CCL}	Both Channels LOW, V_{CC}=5.5V One SDA and one SCL=GND Other SDA and SCL Open		1.5	5	mA
Quiescent Supply Current In Contention	I_{CCAc}	V_{CC}=5.5V, SDAn=SCLn=V_{CC}		1.5	5	mA
INPUT AND OUTPUT SDAB AND SCLB						
HIGH-Level Input Voltage	V_{IH}		0.7 ×V_{CCB}		5.5	V
LOW- Level Input Voltage	V_{IL}	(Note 2)	-0.5		0.3 ×V_{CCB}	V
LOW- Level Input Voltage Contention	V_{ILc}		-0.5	0.4		V
Input Clamping Voltage	V_{IK}	I_I=18mA			-1.2	V
Input Leakage Current	I_{LI}	V_I=5.5V			±1	μA
LOW-Level Input Current	I_{IL}	SDA, SCL, V_I=0.2V			10	μA
LOW-Level Output Voltage	V_{OL}	I_{OL}=100μA or 6mA	0.47	0.52	0.6	V
LOW-Level Input Voltage Below Output LOW-Level Voltage	V_{OL}-V_{ILC}	Guaranteed by design			80	mV
HIGH- Level Output Leakage Current	I_{LOH}	V_O=3.6V			10	μA
Input / Output Capacitance	C_{IO}	V_I=3V or 0V, V_{CC}=3.3V		6		pF
		V_I=3V or 0V, V_{CC}=0V		6		pF

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT AND OUTPUT SDAA AND SCLA						
HIGH-Level Input Voltage	V_{IH}		0.7 ×V_{CCA}		5.5	V
LOW- Level Input Voltage	V_{IL}	(Note 3)	-0.5		0.25 ×V_{CCA}	V
Input Clamping Voltage	V_{IK}	I_I=-18mA			-1.2	V
Input Leakage Current	I_{LI}	V_I=3.6V			±1	uA
LOW-Level Input Voltage	I_{IL}	SDA, SCL, V_I=0.2V			10	uA
LOW- Level Output Voltage	V_{OL}	I_{OL}=6mA		0.1	0.2	V
HIGH-Level Output Leakage Current	I_{LOH}	V_O=3.6V			10	uA
Input/Output Capacitance	C_{IO}	V_I= 3V or 0V, V_{CC}=3.3V		6		pF
		V_I= 3V or 0V, V_{CC}=0V		6		pF
ENABLE						
LOW- Level Input Voltage	V_{IL}		-0.5		0.3 ×V_{CCB}	V
HIGH- Level Input Voltage	V_{IH}		0.7 ×V_{CCB}		5.5	V
LOW- Level Input Current on Pin EN	$I_{IL(EN)}$	V_I=0.2V, EN V_{CC}=3.6V		-10	-30	uA
Input Leakage Current	I_{LI}		-1		+1	uA
Input Capacitance	C_i	V_I =3.0V or 0V		6		pF

Notes: 1. LOW-level supply voltage.

2. V_{IL} specification is for the first LOW level seen by the SDAB/SCLB lines. V_{ILc} is for the second and subsequent LOW levels seen by the SDAB/SCLB lines.
3. V_{IL} for A-side with envelope noise must be below 0.25×V_{CCA} for stable performance.

■ DYNAMIC CHARACTERISTICS

(V_{CC}=2.7V to 5.5V, GND=0V, T_A= −40°C to +85°C, unless otherwise specified) (Note 1, 2)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP (Note 3)	MAX	UNIT
SUPPLIES							
LOW to HIGH Propagation Delay	t_{PLH}	B-side to A-side (Note 4) Figure 1		100	170	250	ns
HIGH to LOW Propagation Delay	t_{PHL}	B-side to A-side Figure 2	V_{CCA} ≤ 2.7V (Note 5)	30	85	110	ns
			V_{CCA} ≥ 3V	10	66	300	ns
LOW to HIGH Transition Time	$t_{t(LH)}$	A-Side, Figure 2		10	130	170	ns
HIGH to LOW Transition Time	$t_{t(HL)}$	A-Side, Figure 2	V_{CCA} ≤ 2.7V (Note 5)	1	22	105	ns
			V_{CCA} ≥ 3V	1	20	175	ns
LOW to HIGH Propagation Delay	t_{PLH}	A-Side to B-side (Note 6) Figure 3		25	53	110	ns
HIGH to LOW Propagation Delay	t_{PHL}	A-Side to B-side (Note 6) Figure 3		60	100	230	ns
LOW to HIGH Transition Time	$t_{t(LH)}$	B-Side, Figure 3		120	140	170	ns
HIGH to LOW Transition Time	$t_{t(HL)}$	B-Side, Figure 3		30	63	90	ns
SET-UP Time	t_{su}	EN HIGH Before START Condition (Note 7)		100			ns
Hold Time	t_h	EN HIGH After STOP Condition (Note 7)		100			ns

Notes: 1. Times are specified with loads of 1.35kΩ pull-up resistance and 57pF load capacitance on the B-side, and 1.35kΩ pull-up resistance and 57pF load capacitance on the A-side. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.

2. Pull-up voltages are V_{CCA} on the A-side and V_{CCB} on the B-side.
3. Typical values were measured with V_{CCA} = 3.3V at T_A=25°C, unless otherwise noted.
4. The t_{PLH} delay data from B-side to A-side is measured at 0.5V on the B-side to 0.5×V_{CCA} on the A-side when V_{CCA} is less than 2V, and 1.5V on the A-side if V_{CCA} is greater than 2V
5. Typical value measured with V_{CCA} = 2.7V at T_A=25°C
6. The proportional delay data from A-side to B-side is measured at 0.25×V_{CCA} on the A-side to 1.5V on the B-side.
7. The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state

■ TEST CIRCUIT AND WAVEFORMS

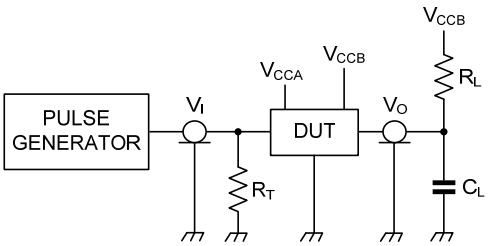


Fig 1. Test Circuit For Open-Drain Output

Notes:
1. R_L= Load Resistor, 1.35kΩ.
C_L = load capacitance includes jig and probe capacitance; 57pF
R_T = termination resistance should be equal to Z_O of pulse generators

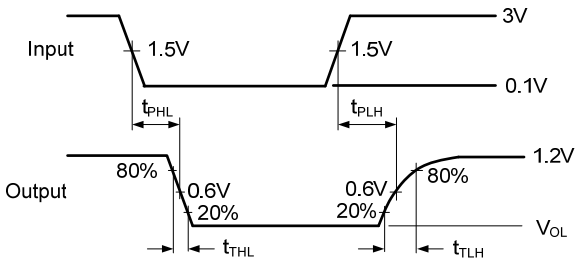


Fig 2. Propagation delay and transition times; Port B to Port A

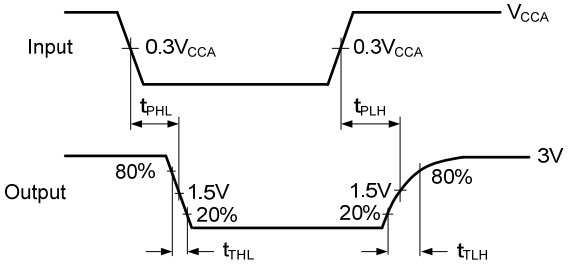


Fig 3. Propagation delay and transition times; Port A to Port B

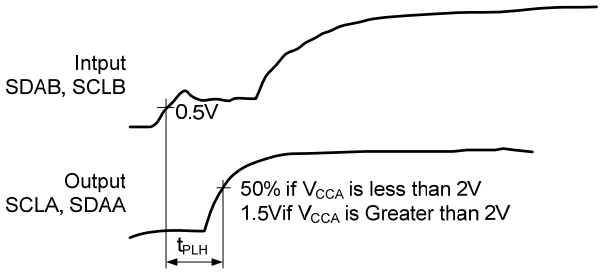


Fig 4. Propagation delay

■ FUNCTIONAL DESCRIPTION

The UTC **UCA9517** enables I^2C-bus or SMBus translation down to V_{CCA} as low as 0.9V without degradation of system performance. The UTC **UCA9517** contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage (as low as 0.9V) and a 3.3V or 5V I^2C-bus or SMBus. All inputs and I/Os are overvoltage tolerant to 5.5 V even when the device is unpowered (V_{CCB} and/or V_{CCA} = 0V). The UTC **UCA9517** includes a power-up circuit that keeps the output drivers turned off until V_{CCB} is above 2.5V and the V_{CCA} is above 0.8V. V_{CCB} and V_{CCA} can be applied in any sequence at power-up. After power-up and with the enable (EN) HIGH, a LOW level on the A-side (below $0.25\times V_{CCA}$) turns the corresponding B-side driver (either SDA or SCL) on and drives the B-side down to about 0.5V. When the A-side rises above $0.25\times V_{CCA}$ the B-side pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When the B-side falls first and goes below $0.3\times V_{CCB}$ the A-side driver is turned on and the A-side pulls down to 0 V. The B-side pull-down is not enabled unless the B-side voltage goes below 0.4V. If the B-side low voltage does not go below 0.5V, the A-side driver will turn off when the B-side voltage is above $0.7\times V_{CCB}$. If the B-side low voltage goes below 0.4V, the B-side pull-down driver is enabled and the B-side will only be able to rise to 0.5V until the A-side rises above $0.25\times V_{CCA}$, then the B-side will continue to rise being pulled up by the external pull-up resistor. The V_{CCA} is only used to provide the $0.25\times V_{CCA}$ reference to the A-side input comparators and for the power good detect circuit. The UTC **UCA9517** logic and all I/Os are powered by the V_{CCB} pin.

Enable

The EN pin is active HIGH with an internal pull-up to V_{CCB} and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I^2C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I^2C-bus parts being enabled.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

I^2C-bus systems

As with the standard I^2C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I^2C-bus).The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with Standard mode and Fast mode I^2C-bus devices in addition to SMBus devices. Standard mode I^2C-bus devices only specify 3mA output drive; this limits the termination current to 3mA in a generic I^2C-bus system where Standard mode devices and multiple masters are possible. Under certain conditions higher termination currents can be used.

■ TYPICAL APPLICATION CIRCUIT

A typical application is shown in Figure 5. In this example, the system master is running on a 3.3V I^2C-bus while the slave is connected to a 1.2V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

The UTC **UCA9517** is 5V tolerant, so it does not require any additional circuitry to translate between 0.9V to 5.5V bus voltages and 2.7V to 5.5V bus voltages. When the A-side of the UTC **UCA9517** is pulled LOW by a driver on the I^2C-bus, a comparator detects the falling edge when it goes below $0.25\times V_{CCA}$ and causes the internal driver on the B-side to turn on, causing the B-side to pull down to about 0.5V. When the B-side of the UTC **UCA9517** falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on the A-side to turn on and pull the A-side pin down to ground.

On the B bus side of the UTC **UCA9517**, the clock and data lines would have a positive offset from ground equal to the VOL of the UTC **UCA9517**. After the 8th clock pulse, the data line will be pulled to the V_{OL} of the slave device which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the UTC **UCA9517** for a short delay while the A bus side rises above $0.25\times V_{CCA}$ then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the UTC **UCA9517** (V_{IL}) be at or below 0.4V to be recognized by the UTC **UCA9517** and then transmitted to the A bus side.

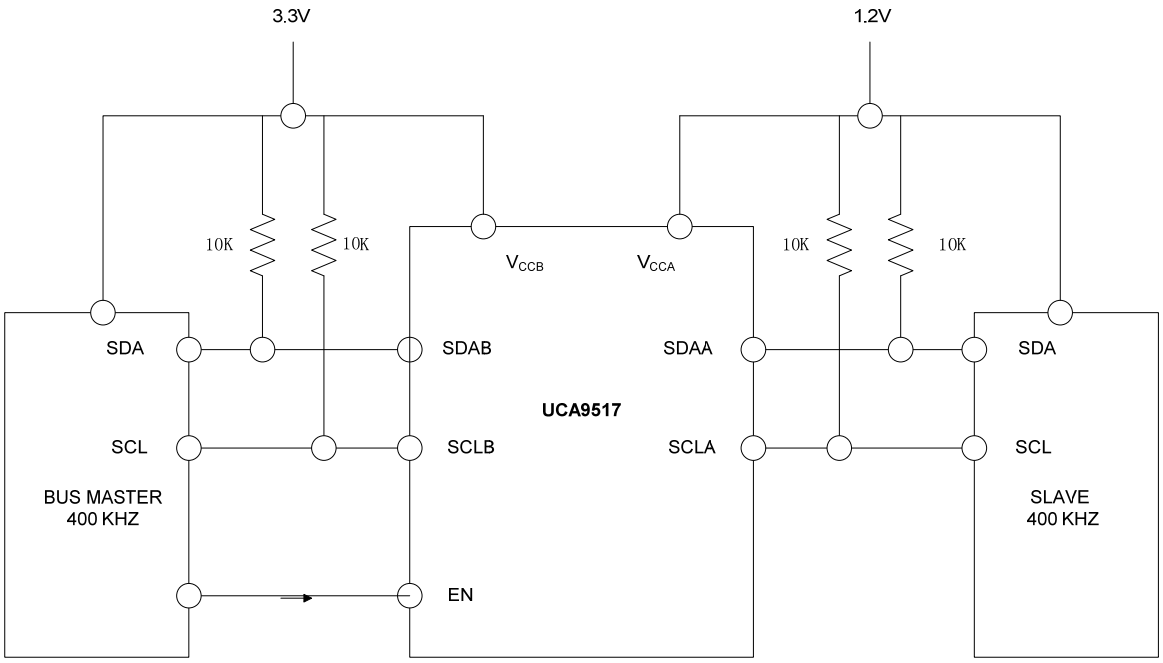


Fig5. Typical Application