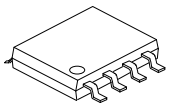
I²C COMPATIBLE DUAL BIDIRECTIONAL BUS BUFFER



SOP-8

■ DESCRIPTION

The UTC **UMX82B96** is a bus buffer that supports bidirectional data transfer between an I²C bus and a range of other bus configurations with different voltage and current levels.

One of the advantages of the UTC **UMX82B96** is that it supports longer cables/traces and allows for more devices per I²C bus because it can isolate bus capacitance such that the total loading (devices and trace lengths) of the new bus or remote I²C nodes are not apparent to other I²C buses (or nodes). The restrictions on the number of I²C devices in a system due to capacitance, or the physical separation between them, are greatly improved.

The device is able to provide galvanic isolation (optocoupling) or use balanced transmission lines (twisted pairs), because separate directional Tx and Rx signals are provided. The Tx and Rx signals may be connected directly (without causing bus latching), to provide an bidirectional signal line with I²C properties (open-drain driver). Likewise, the Ty and Ry signals may also be connected together to provide an bidirectional signal line with I²C properties (open-drain driver). This allows for a simple communication design, saving design time and costs.

■ FEATURES

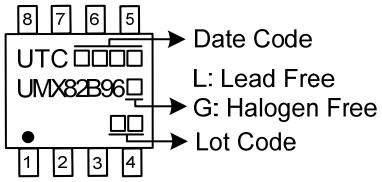
* Operating Power-Supply Voltage Range of 2V to 15V
* Can Interface Between I²C Buses Operating at Different Logic Levels (2V to 15V)
* Outputs on the Transmission Side (Tx/Ty) Have High Current Sink Capability for Driving Low-Impedance or High-Capacitive Buses
* Interface With Optoelectrical Isolators and Similar Devices That Need Unidirectional Input and Output Signal Paths by Splitting I²C Bus Signals Into Pairs of Forward (Tx/Ty) and Reverse (Rx/Ry) Signals
* 400-kHz Fast I²C Bus Operation Over at Least 20 Meters of Wire

■ ORDERING INFORMATION

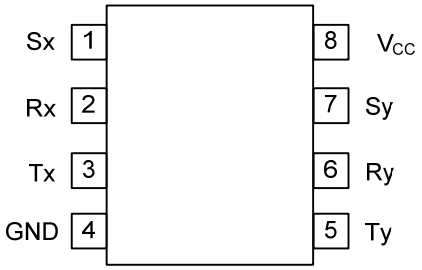
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UMX82B96L-S08-R	UMX82B96G-S08-R	SOP-8	Tape Reel

UMX82B96G-S08-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



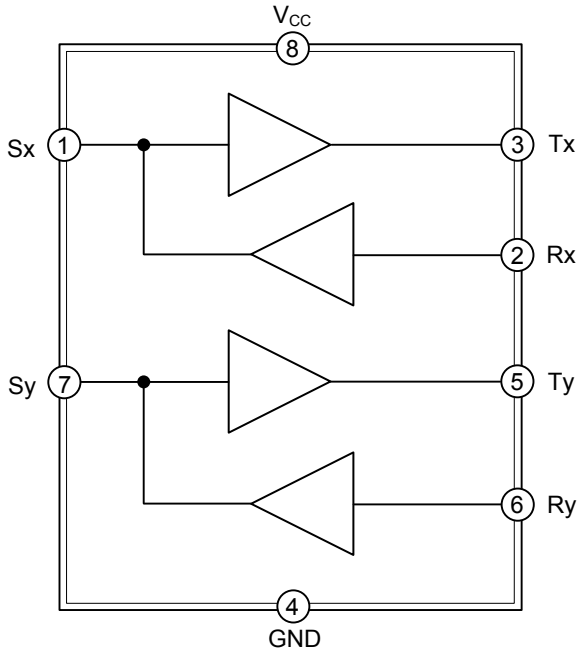
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	Sx	Serial data bus or SDA. Connect to V_{CC} of I^2C master through a pull up resistor.
2	Rx	Receive signal. Connect to V_{CC} of UTC **UMX82B96** through a pull up resistor.
3	Tx	Transmit signal. Connect to V_{CC} of UTC **UMX82B96** through a pull up resistor.
4	GND	Ground
5	Ty	Transmit signal. Connect to V_{CC} of UTC **UMX82B96** through a pull up resistor.
6	Ry	Receive signal. Connect to V_{CC} of UTC **UMX82B96** through a pull up resistor.
7	Sy	Serial clock bus or SCL. Connect to V_{CC} of I^2C master through a pull up resistor.
8	V_{CC}	Supply voltage

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified.)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage on V_{CC} Pin		V_{CC}	-0.3 ~ 18	V
Voltage on Buffered Input	Sx or Sy (SDA or SCL)	V_I	-0.3 ~ 18	V
	Rx or Ry		-0.3 ~ 18	V
Voltage on Buffered Output	Sx or Sy (SDA or SCL)	V_O	-0.3 ~ 18	V
	Tx or Ty		-0.3 ~ 18	V
Continuous Output Current	Sx or Sy	I_O	250	mA
	Tx or Ty		250	mA
Continuous Current through V_{CC} or GND		I_{CC}	250	mA
Operating Free-Air Temperature		T_A	-40 ~ +85	°C
Storage Temperature		T_{STG}	-55 ~ +165	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER			SYMBOL	T_A=25°C			UNIT
				MIN	TYP	MAX	
Supply Voltage			V_{CC}	2		15	V
Low-Level Output Current	Sx, Sy	V_{Sx}, V_{Sy}=1V, V_{Rx}, V_{Ry} ≤ 0.42V	I_{OL}			3	mA
	Tx, Ty	V_{Sx}, V_{Sy}=0.4V, V_{Tx}, V_{Ty}=0.4V				30	mA
Maximum Input/Output Voltage Level	Sx, Sy	V_{Tx}, V_{Ty}=0.4V	V_{IOmax}			15	V
	Tx, Ty	V_{Sx}, V_{Sy}=0.4V				15	V
Low-Level Input Voltage Difference	Sx, Sy		V_{ILdiff}			0.4	V

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	120	°C/W

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.3V ~ 5.5V, 15V, voltages are specified with respect to GND, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS		T_A=25°C			T_A=-40~+85°C			UNIT
					MIN	TYP (Note 1)	MAX	MIN	TYP	MAX	
Temperature Coefficient of Input Thresholds	Sx, Sy	$\Delta V/\Delta T_{IN}$				-2			-2		mV/°C
Low-Level Output Voltage	Sx, Sy	V_{OL}	I_{Sx}, I_{Sy}=3mA		0.75	0.88	1	0.6		1.1	V
			I_{Sx}, I_{Sy}=0.2mA		0.6	0.73	0.8	0.5		0.9	V
Temperature Coefficient of Output Low Levels (Note 2)	Sx, Sy	$\Delta V/\Delta T_{OUT}$	I_{Sx}, I_{Sy}=0.2mA			-1.8			-1.8		mV/°C
Quiescent Supply Current		I_{CC}	Sx=Sy=V_{CC}			0.9	1.8			2	mA
Additional Supply Current Per Pin Low	Tx, Ty	ΔI_{CC}				1.7	2.75			3	mA
Dynamic Output Sink Capability on I^2C Bus Leakage Current on I^2C Bus	Sx, Sy	I_{IOS}	V_{Sx}, V_{Sy}>2V, V_{Rx}, V_{Ry}=Low		7	20		5.5			mA
			V_{Sx}, V_{Sy}=2.5V V_{Rx}, V_{Ry}=High	V_{CC}=2.3V~2.7V		0.1	1			1	µA
			V_{Sx}, V_{Sy}=5V	V_{CC}=3V~3.6V		0.1	1			1	µA
			V_{Rx}, V_{Ry}=High	V_{CC}=4.5V~5.5V		0.1	1			1	µA
			V_{Sx}, V_{Sy}=15V V_{Rx}, V_{Ry}=High	V_{CC}=15V		0.1	1			1	µA
Dynamic Output Sink Capability on Buffered Bus	Tx, Ty	I_{IOT}	V_{Tx} , V_{Ty}>1V, V_{Sx}, V_{Sy}=Low On I^2Cbus=0.4V		60	80		60			mA
Leakage Current on Buffered Bus			V_{Tx}, V_{Ty} =V_{CC}=2.5V, V_{Sx}, V_{Sy}=High	V_{CC}=2.3V~2.7V		0.1	1			1	µA
			V_{Tx}, V_{Ty} =V_{CC}=3.3V, V_{Sx}, V_{Sy}=High	V_{CC}=3V~3.6V		0.1	1			1	µA
			V_{Tx}, V_{Ty} =V_{CC}=5V, V_{Sx}, V_{Sy}=High	V_{CC}=4.5V~5.5V		0.1	1			1	µA
			V_{Tx}, V_{Ty} =V_{CC}=15V, V_{Sx}, V_{Sy}=High	V_{CC}=15V		0.1	1			1	µA
Input Current from I^2C Bus	Sx, Sy	I_I	Bus Low, V_{Rx}, V_{Ry}=High			-1				1	µA
Input Current from Buffered Bus	Rx, Ry		Bus Low, V_{Rx}, V_{Ry}=0.4V			-1				1	µA
Leakage Current on Buffered Bus Input			V_{Rx}, V_{Ry}=V_{CC}			-1				1.5	µA

■ ELECTRICAL CHARACTERISTICS (Cont.)

(V_{CC} = 2.3V ~ 5.5V, 15V, voltages are specified with respect to GND, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	T_A=25°C			T_A=-40~+85°C			UNIT
				MIN	TYP (Note 1)	MAX	MIN	TYP	MAX	
Input Threshold	Sx, Sy	V_{IT}	Input Logic Level High Threshold (Note 3) on Normal I^2C Bus		0.65	0.85			0.9	V
			Input Logic Level Low Threshold (Note 3) on Normal I^2C Bus	0.6	0.65		0.3			V
	Rx, Ry		Input Logic Level High	0.58× V_{CC}			0.58× V_{CC}			V
			Input Threshold		0.5× V_{CC}					V
			Input Logic Level Low			0.42× V_{CC}			0.42× V_{CC}	V
Input/Output Logic Level Difference (Note 4)	Sx, Sy	V_{IOdiff}	(V_{Sx} Output Low at 3mA) – (V_{Sx} Input High Max) for I^2C Applications	100	150		100			mV
V_{CC} Voltage at which all Buses are Released	Sx, Sy Tx, Ty	V_{IOrel}	Sx, Sy are Low, V_{CC} Ramping, Voltage on Tx, Ty Lowered until Released	1			1			V
Temperature Coefficient of Release Voltage		$\Delta V/\Delta T_{REL}$			-4			-4		mV/°C
Input Capacitance	Rx, Ry	C_{IN}			2.5	4			4	pF

Notes: 1. Typical value is at V_{CC} = 2.5V, T_A =25°C.

2. The output logic low depends on the sink current.
3. The input logic threshold is independent of the supply voltage.
4. The minimum value requirement for pullup current, 200μA, ensures that the minimum value for V_{SX} output low always exceeds the minimum V_{Sx} input high level to eliminate any possibility of latching. The specified difference is specified by design within any device.While the tolerances on absolute levels allow a small probability that the low from one Sx output is recognized by an Sx input of another.
   UTC **UMX82B96**, this has no consequences for normal applications.

■ SWITCHING CHARACTERISTICS

(V_{CC} = 5V, T_A =25°C, no capacitive loads, voltages are specified with respect to GND, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Buffer Delay Time On Falling Input for Input V_{Sx} (or V_{Sy}) = Input Switching Threshold to Output V_{Tx} (or V_{Ty}) Output Falling 50% of V_{LOAD} (Note 1)	t_{pzl}	R_{Tx} Pullup = 160Ω, C_{Tx} = 7pF + Board Trace Capacitance		90		ns
Buffer Delay Time On Rising Input for Input V_{Sx} (or V_{Sy}) = Input Switching Threshold to Output V_{Tx} (or V_{Ty}) Output Reaching 50% of V_{LOAD} (Note 2)	t_{plz}	R_{Tx} Pullup = 160Ω, C_{Tx} = 7pF + Board Trace Capacitance		30		ns
Buffer Delay Time On Falling Input for Input V_{Rx} (or V_{Ry}) = Input Switching Threshold to Output V_{Sx} (or V_{Sy}) Output Falling 50% of V_{LOAD} (Note 3)	t_{pzl}	R_{Sx} Pullup = 1500Ω, C_{Tx} = 7pF + Board Trace Capacitance		150		ns
Buffer Delay Time On Rising Input for Input V_{Rx} (or V_{Ry}) = Input Switching Threshold to Output V_{Sx} (or V_{Sy}) Output Reaching 50% of V_{LOAD} (Note 4)	t_{plz}	R_{Sx} Pullup = 1500Ω, C_{Tx} = 7pF + Board Trace Capacitance		150		ns

Notes: 1. The fall time of V_{Tx} from 5V to 2.5V in the test is approximately 15ns.
2. The rise time of V_{Tx} from 0V to 2.5V in the test is approximately 20ns.
3. The fall time of V_{Sx} from 5V to 2.5V in the test is approximately 50ns.
4. The rise time of V_{Sx} from 0.9V to 2.5V in the test is approximately 70ns.

■ TYPICAL APPLICATION CIRCUIT

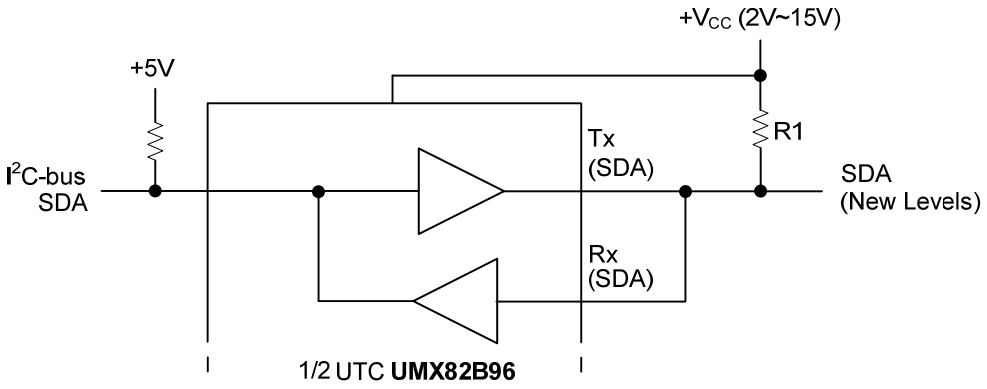


Fig. 1 Interfacing an I^2C Type of Bus With Different Logic Levels

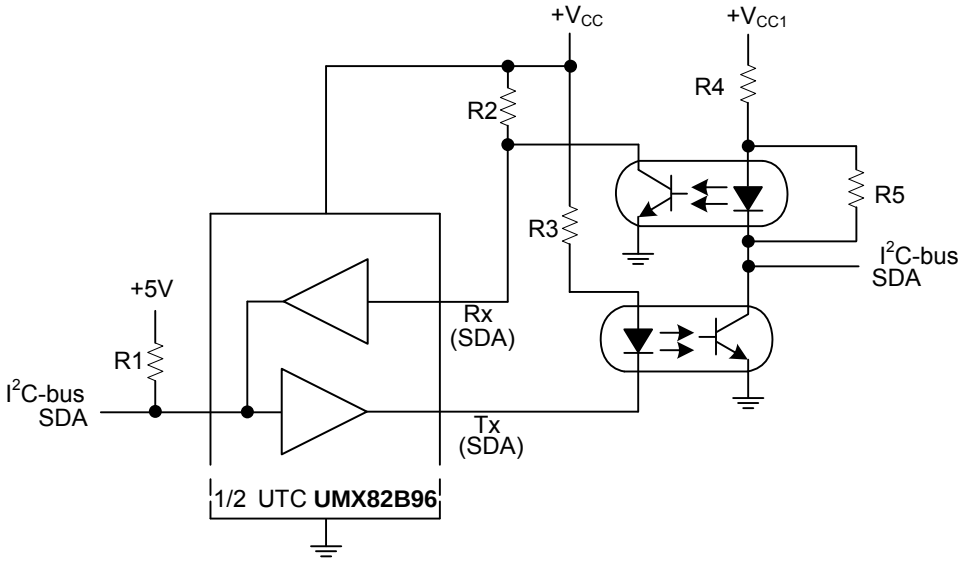


Fig. 2 Galvanic Isolation of I^2C-Bus Nodes via Opto-Couplers

■ TYPICAL APPLICATION CIRCUIT (Cont.)

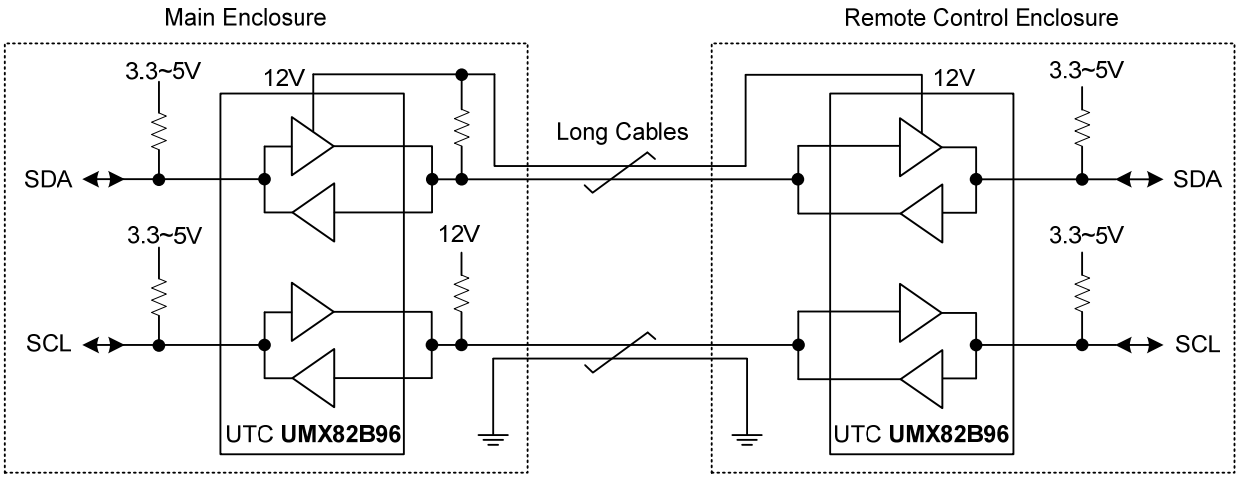


Fig. 3 Long-Distance I^2C-Bus Communications