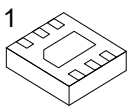
LOW-POWER, PUSH-BUTTON CONTROLLERS WITH CONFIGURABLE DELAY



X2DFN1616-6

■ DESCRIPTION

The UTC **83NXX** are low-current, ultrasmall, push-button reset timers. These devices use a long timing setup delay to provide the intended system reset, and avoid resets from short push-button closures or key presses. This reset configuration also allows for differentiation between software interrupts and hard system resets.

The UTC **83N20** monitors two inputs (PB1 and PB2) and output an active-low reset pulse signal ($\overline{RST}$) when both inputs are low for the selected time delay. For the UTC **83N20**, $\overline{RST}$ remains low until one of the PBx inputs is released. The need for a dedicated reset button is eliminated because two inputs are used to ensure reset. The UTC **83N22** monitors one input (PB1) and outputs an active-low reset pulse signal ($\overline{RST}$) when PB1 is low for the selected time delay.

The UTC **83NXX** have an open-drain output that can be wire-ORed with other open-drain devices. The UTC **83NXX** operate from 1.6V to 6.5V over the -40°C to +105°C temperature range, and provide a precise, space-conscious micropower solution for system resetting needs.

■ FEATURES

* Operating Range: 1.6V ~ 6.5V
* Single (UTC **83N22**) or Dual (UTC **83N20**) Push-Button Inputs
* Low Supply Current: 400nA (Typical)
* Two-State Logic, User-Selectable Input Delay:
  -For Example: 7.5s and 0s
  -Multiple Timing Options Available
* Fixed Time-out Pulse at $\overline{RST}$: 400ms (Typical)
  -Other Timing Options Available on Request
* Active Low, Open-Drain Output

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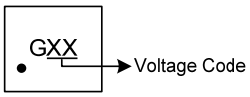
■ ORDERING INFORMATION

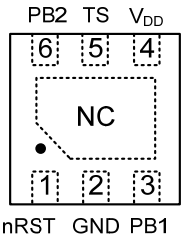
Ordering Number		Package	Packing
Lead Free	Halogen Free		
83NXXL-K06-1616-R	83NXXG-K06-1616-R	X2DFN1616-6	Tape Reel

83NXXG-K06-1616-R (1)Packing Type (2)Package Type (3)Green Package (4)Output Voltage Code	(1) R: Tape Reel (2) K06-1616: X2DFN1616-6 (3) G: Halogen Free and Lead Free, L: Lead Free (4) XX: refer to Marking Information

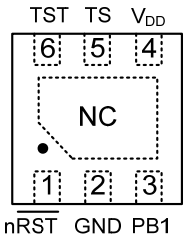
■ MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
X2DFN1616-6	20: 2.0V 22: 2.2V	

■ PIN CONFIGURATION



83N20
(TOP VIEW)



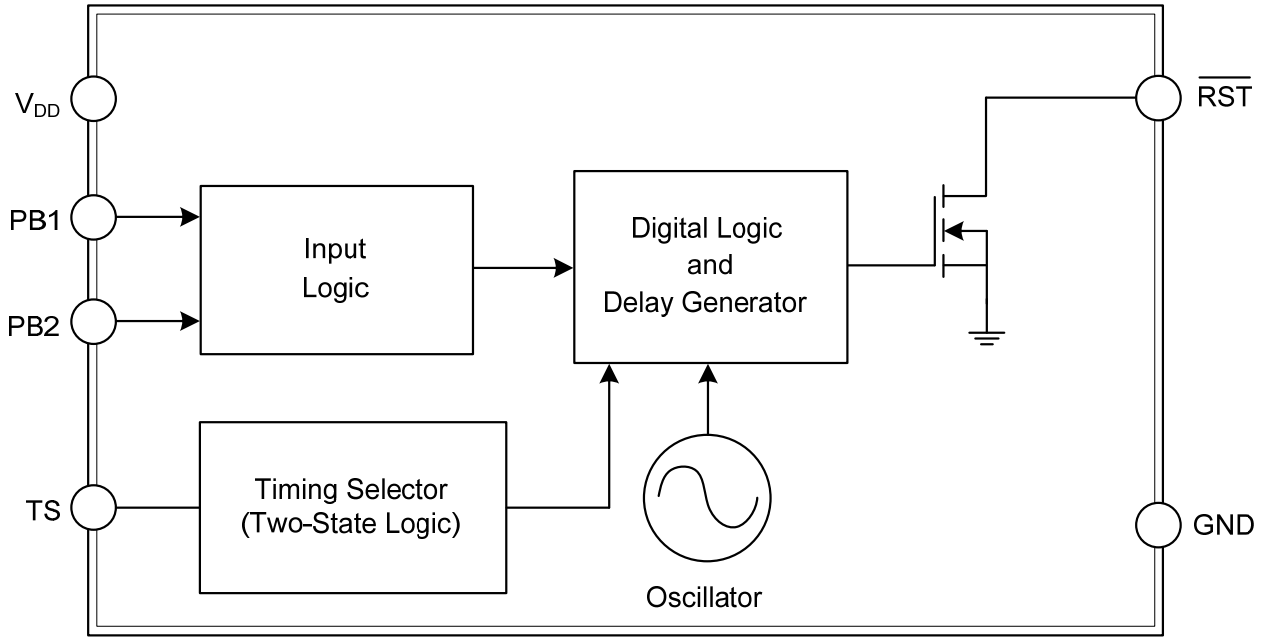
83N22
(TOP VIEW)

■ PIN DESCRIPTION

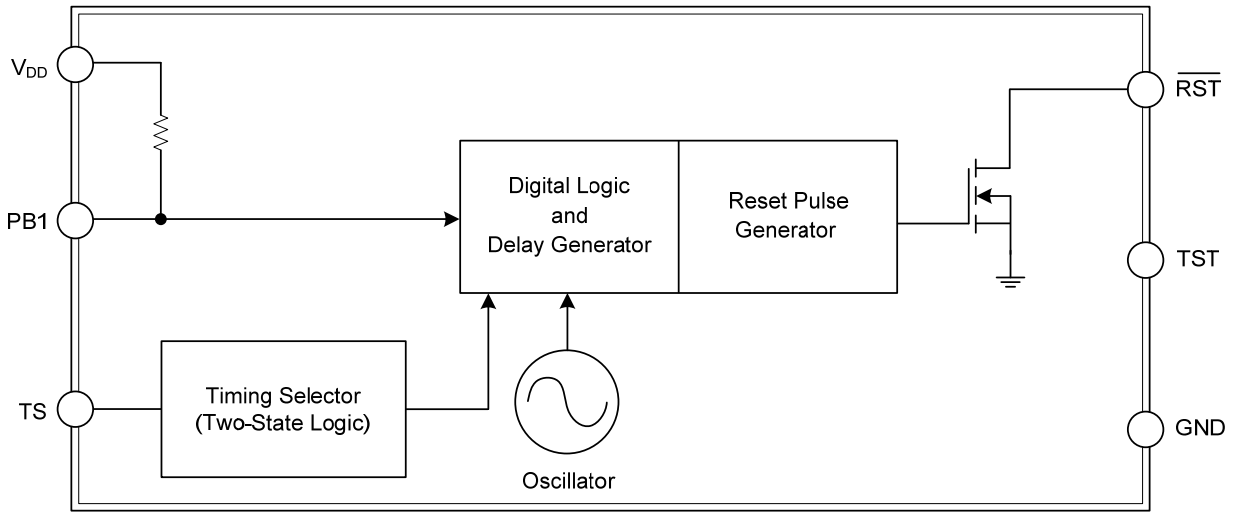
PIN NO.	PIN NAME	DESCRIPTION
1	$\overline{RST}$	Active low, open-drain output. Reset is asserted (goes low) when both PB1 and PB2 are held low for longer than t_{TIMER} time (only PB1 for UTC **83N22**). Reset is deasserted when either PBx input goes high.
2	GND	Ground.
3	PB1	Push-button input. PB1 and PB2 must be held low for greater than t_{TIMER} time to assert the reset output.
4	V_{DD}	Supply voltage input. Connect a 1.6V to 6.5V supply to V_{DD} to power the device. It is good analog design practice to place a 0.1μF ceramic capacitor close to this pin.
5	TS	Time delay selection input. Connect to V_{DD} or GND for different t_{TIMER} selections. In normal operation, the TS pin state should not be changed because it is intended to be permanently connected to either GND or V_{DD}. If switching the TS pin is required, it should be done during power off, or when either PBx input is high.
6 (83N20)	PB2	Second push-button input. PB1 and PB2 must be held low for greater than t_{TIMER} time to assert the reset output.
6 (83N22)	TST	Connect this pin to GND or V_{DD} during normal device operation.
Exposed Pad	NC	Thermal pad.

■ BLOCK DIAGRAM

83N20



83N22



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.3 ~ 7	V
$\overline{RST}$ Voltage	$V_{\overline{RST}}$	-0.3 ~ 7	V
PB1, PB2 Voltage	V_{PB1}, V_{PB2}	-0.3 ~ 7	V
TS Voltage	V_{TS}	-0.3 ~ V_{DD} + 0.3	V
$\overline{RST}$ Current	$I_{\overline{RST}}$	±20	V/ns
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS
Power-Supply Voltage	V_{DD}	1.6		6.5	V
SENSE Voltage	V_{TS}	0		V_{DD}	V
$\overline{RESET}$ Pin Voltage	V_{PB1}, V_{PB2}	0		6.5	V
RST Pin Voltage	V_{RST}	0		6.5	V
RST Pin Current	I_{RST}	0.00035		8	mA

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	360	°C/W

■ ELECTRICAL CHARACTERISTICS

($1.6V \le V_{DD} \le 6.5V$, Typical values are T_A=25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Supply	V_{DD}			1.6		6.5	V
Supply Current (Standby)	I_{CC}	V_{DD}=3.3V	83N22		400		nA
		V_{DD}=6.5V				3.3	μA
		V_{DD}=3.3V	83N20		350		nA
		V_{DD}=6.5V				3.4	μA
Supply Current (Active Timer) (Note 1)		PB1, PB2=0V, V_{DD}=6.5V	83N20		1	12	μA
		PB1=0V, V_{DD}=6.5V	83N22		30	136	μA
High-Level Input Voltage	V_{IH}	PB1	83N22	0.7 ×V_{DD}			V
		PB1, PB2	83N20	0.85			V
Low-Level Input Voltage	V_{IL}	PB1	83N22	0		0.35	V
		PB1, PB2	83N20	0		0.35	V
Input Current (PB1, PB2)	I_{PB}	PB1, PB2 = 0V or V_{DD}	83N20	-50		50	nA
		PB1=V_{DD}	83N22	-50		50	nA
Low-Level Output Voltage	V_{OL}	$V_{DD} \ge 4.5V$, I_{SINK}=8mA				0.4	V
		$V_{DD} \ge 3.3V$, I_{SINK}=5mA				0.3	V
		$V_{DD} \ge 1.6V$, I_{SINK}=3mA				0.8	V
Open-Drain Output Leakage Current	$I_{lkg(OD)}$	High Impedance, $V_{\overline{RST}}$ =6.5V		-0.35		0.35	μA

Note: Includes current through pullup resistor between input pin (PB1) and supply pin (V_{DD}) for UTC **83N22**.

■ TIMING REQUIREMENTS

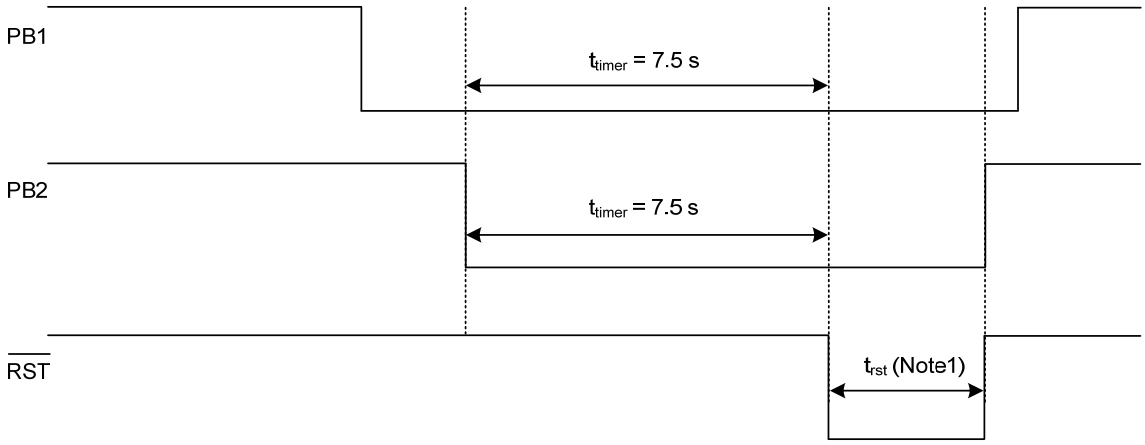
All specifications are over the operating temperature range of -40°C < T_J < 125°C and 1.6V ≤ V_{DD} ≤ 6.5V, unless otherwise noted. Typical values are at T_J = 25°C and V_{DD} = 3.3V.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Push-Button Timer (Note1)	t_{TIMER}			-20		20	%
		TS=GND	83N20	6	7.5	9	s
		TS=V_{DD}		10	12.5	15	s
		TS=GND	83N22	6	7.5	9	s
		TS=V_{DD}			0		s
Reset Pulse Duration	t_{RST}			-20		20	%
		UTC 83N22		320	400	480	ms
Detection Delay (from Input to $\overline{RST}$) (Note 2)	t_{DD}	For 0-s t_{TIMER} Condition			150		μs
Start-up Delay (Note 2)	t_{SD}	V_{DD} Rising			300		μs

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. For devices with a 0-second delay when TS = V_{DD}, reset asserts in t_{DD} time when both PB inputs go low in this configuration. During start-up, if the PB inputs are low, reset asserts after a start-up time delay. This value is specified by design.

■ TIMING DIAGRAM



Note 1. For the UTC **83N20**, t_{RST} is not a fixed time, but instead depends on one of the PB pins going high.

Figure 1. UTC **83N20** Timing Diagram

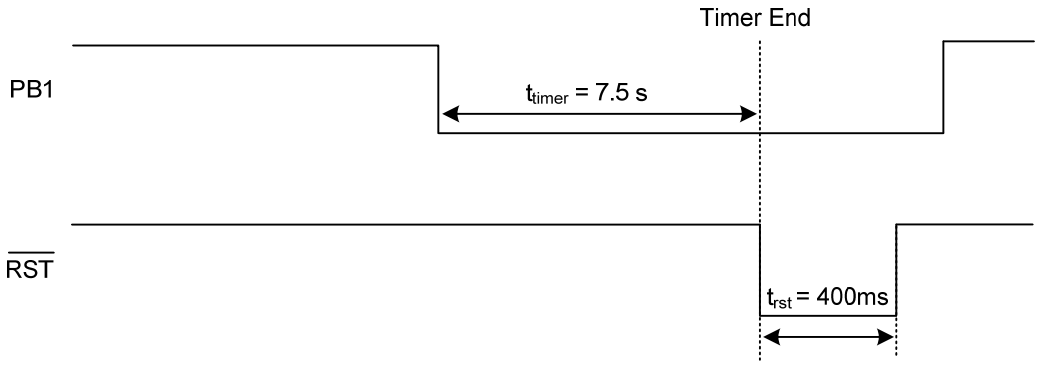
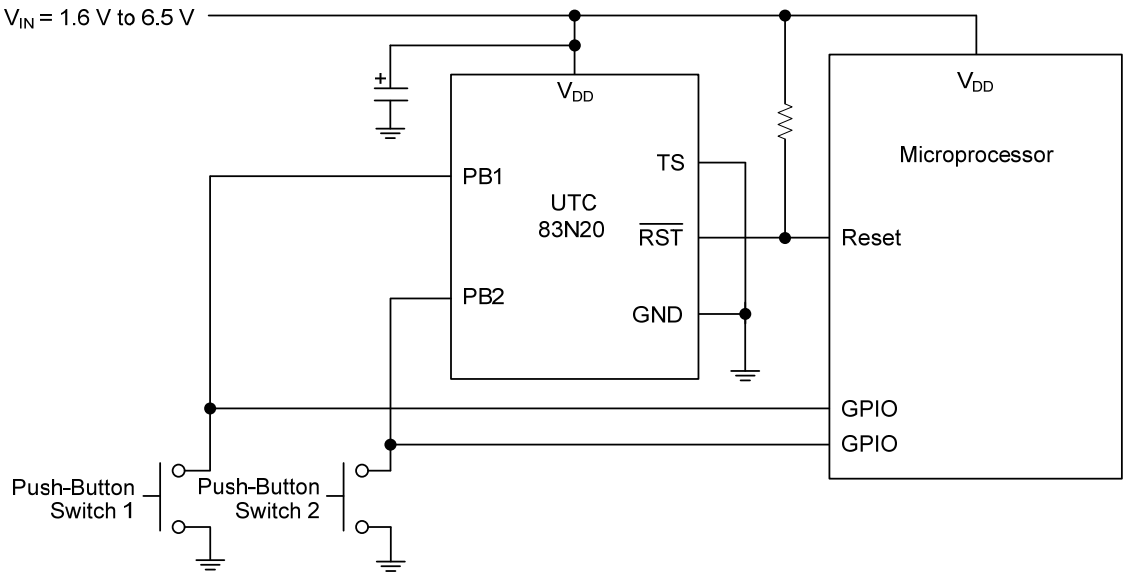


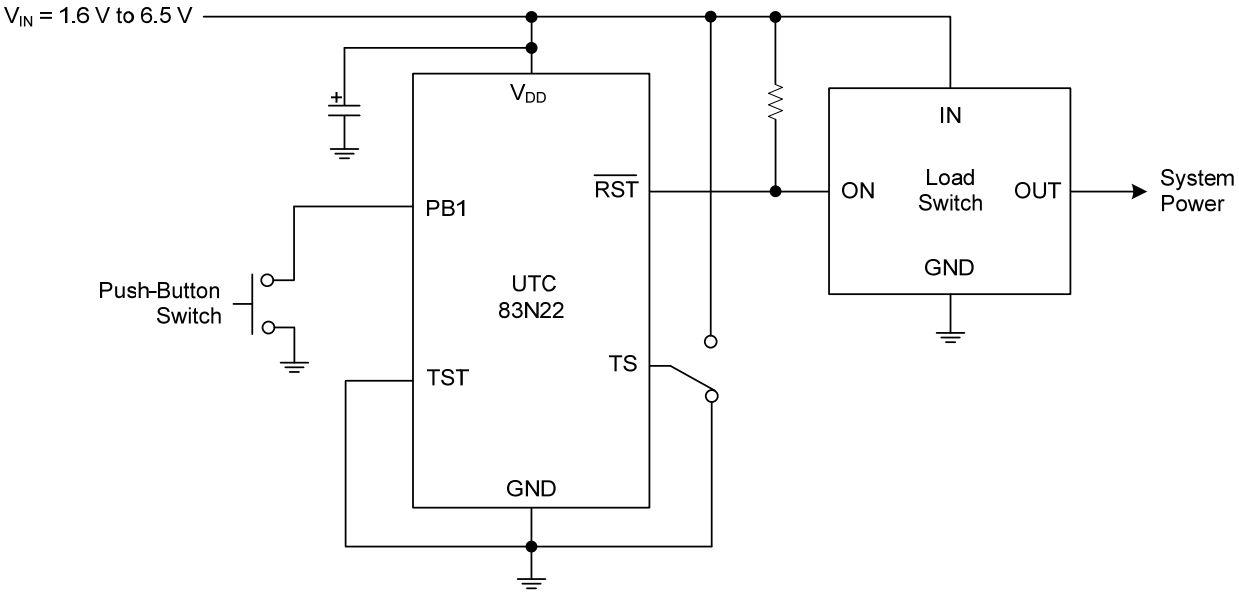
Figure 2. UTC **83N22** Timing Diagram

■ TYPICAL APPLICATION CIRCUIT



Note: Connect TS to V_{CC} or ground for different PB time delays. Connect one PB input to ground for use as a single channel.

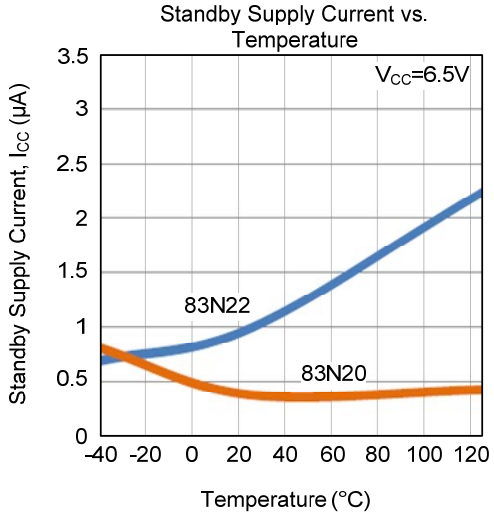
Figure 3. UTC **83N20** Application Diagram

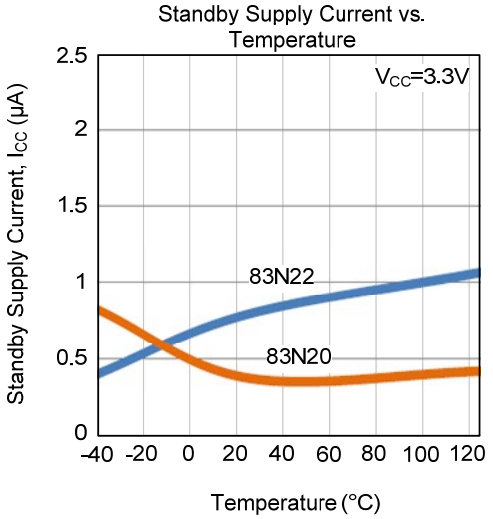


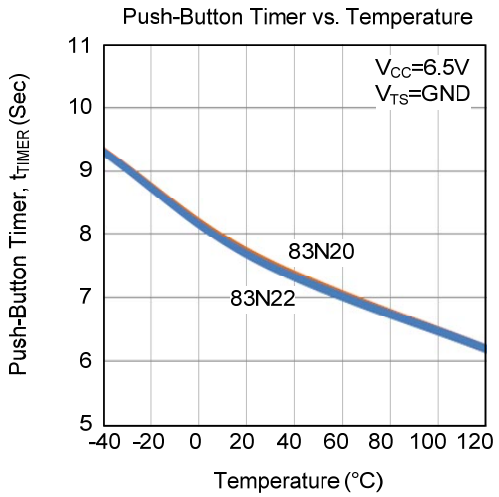
Note: Connect TS to V_{DD} or ground for different PB time delays.

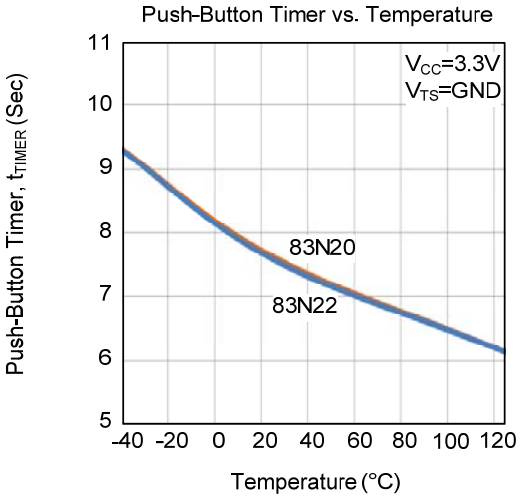
Figure 6. UTC **83N22** Application Diagram

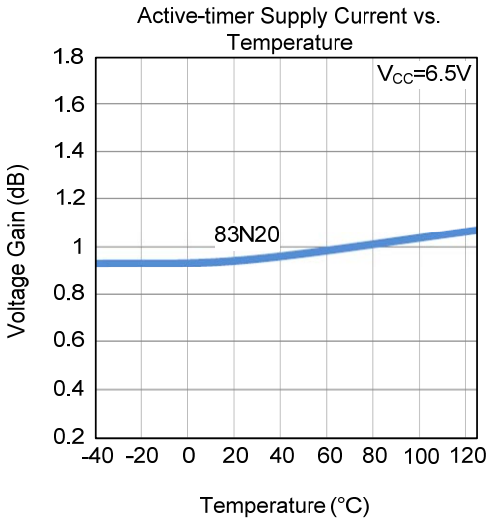
■ TYPICAL CHARACTERISTICS

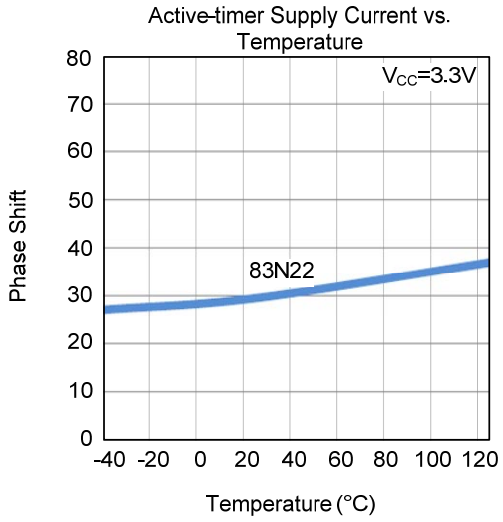












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