



U74LVC00B

CMOS IC

QUAD 2-INPUT NAND GATE

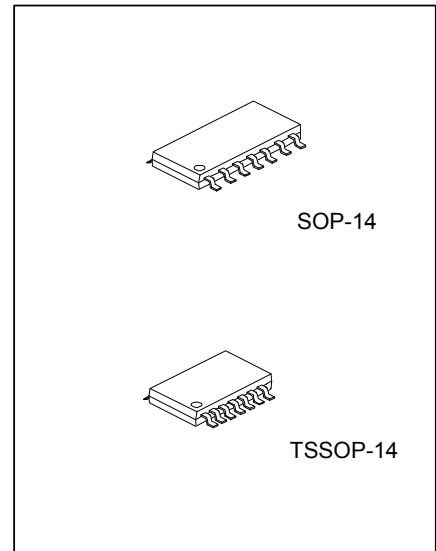
DESCRIPTION

The **U74LVC00B** is a quad 2-input NAND gate which performs the Function $Y=A \bullet B$ or $Y=\overline{A + B}$ in positive logic circuit.

This device has power-down protective circuit to prevent the device from destruction when it is powered down.

FEATURES

- * Operate From 1.65V to 3.6V
- * Inputs Accept Voltages to 5.5V
- * High Noise Immunity
- * Low Power Dissipation
- * Max t_{PD} of 5 ns at 3.3V



ORDERING INFORMATION

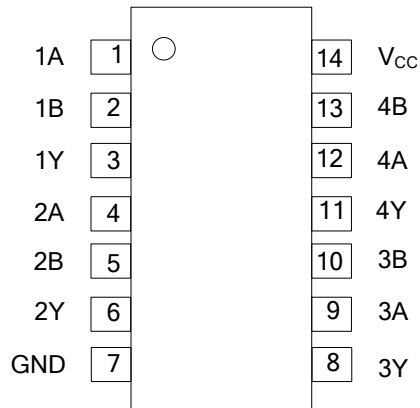
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC00BL-S14-R	U74LVC00BG-S14-R	SOP-14	Tape Reel
U74LVC00BL-P14-R	U74LVC00BG-P14-R	TSSOP-14	Tape Reel

<p>U74LVC00BG-S14-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) S14: SOP-14, P14: TSSOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING

SOP-14	TSSOP-14
<p> 14 13 12 11 10 9 8 → Date Code UTC □ □ □ □ → L: Lead Free U74LVC00B □ → G: Halogen Free ● □ □ □ → Lot Code 1 2 3 4 5 6 7 </p>	<p> 14 13 12 11 10 9 8 → Date Code UTC □ □ □ □ → L: Lead Free U74LVC00B □ → G: Halogen Free ● □ □ □ → Lot Code 1 2 3 4 5 6 7 </p>

■ PIN CONFIGURATION

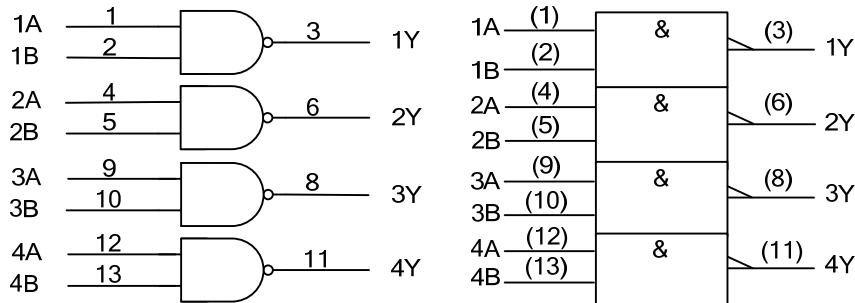


■ FUNCTION TABLE

INPUT(nA)	INPUT(nB)	OUTPUT(nY)
H	H	L
H	L	H
L	H	H
L	L	H

Note: H: HIGH voltage level; L: LOW voltage level.

■ LOGIC DIAGRAM (Positive Logic)



Logic Symbol

IEC Logic Symbol

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 6.5	V
Input Voltage	V_{IN}	-0.5 ~ 6.5	V
Output Voltage	V_{OUT}	-0.5 ~ $V_{CC}+0.5$	V
V_{CC} or GND Current (Output In The Power-Off State)	I_{CC}	±100	mA
Continuous Output Current ($V_{OUT}=0$ to V_{CC})	I_{OUT}	±50	mA
Input Clamp Current ($V_{IN}<0$)	I_{IK}	-50	mA
Output Clamp Current ($V_{OUT}<0$ or $V_{OUT}>V_{CC}$)	I_{OK}	-50	mA
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		3.6	V
High-Level Input Voltage	V_{IH}	$V_{CC}=1.65V$ to $1.95V$	$0.65 \times V_{CC}$			V
		$V_{CC}=2.3V$ to $2.7V$	1.7			
		$V_{CC}=2.7V$ to $3.6V$	2			
Low-Level Input Voltage	V_{IL}	$V_{CC}=1.65V$ to $1.95V$			$0.35 \times V_{CC}$	V
		$V_{CC}=2.3V$ to $2.7V$			0.7	
		$V_{CC}=2.7V$ to $3.6V$			0.8	
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Ambient Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
High-Level Output Voltage	V_{OH}	$I_{OH}=-100\mu A$, $V_{CC}=1.65V$ to $3.6V$	$V_{CC}-0.2$			V	
		$I_{OH}=-4mA$, $V_{CC}=1.65V$	1.2			V	
		$I_{OH}=-8mA$, $V_{CC}=2.3V$	1.7			V	
		$I_{OH}=-12mA$	$V_{CC}=2.7V$	2.2			V
			$V_{CC}=3V$	2.4			
		$I_{OH}=-24mA$	$V_{CC}=3.0V$	2.2			V
Low-Level Output Voltage	V_{OL}	$I_{OL}=100\mu A$, $V_{CC}=1.65V$ to $3.6V$			0.2	V	
		$I_{OL}=4mA$, $V_{CC}=1.65V$			0.45	V	
		$I_{OL}=8mA$, $V_{CC}=2.3V$			0.7	V	
		$I_{OL}=12mA$, $V_{CC}=2.7V$			0.4	V	
		$I_{OL}=24mA$, $V_{CC}=3.0V$			0.55	V	
Input Leakage Current	$I_{I(LEAK)}$	$V_{IN}=5.5V$ or GND, $V_{CC}=3.6V$			±5	μA	
Quiescent Supply Current	I_Q	$V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$, $V_{CC}=3.6V$			10	μA	
Additional Quiescent Supply Current Per Input Pin	ΔI_Q	$V_{CC}=2.7 \sim 3.6V$, One input at $V_{CC}-0.6V$, Other inputs at V_{CC} or GND, $I_{OUT}=0$			500	μA	
Input Capacitance	C_{IN}	$V_{IN}=V_{CC}$ or GND		5		pF	

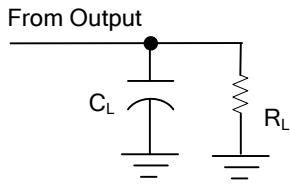
■ SWITCHING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From Input (nA or nB) To Output (nY)	t _{PD}	V _{CC} =2.7V, R _L =500Ω	1.0		5.1	ns
		V _{CC} =3.3±0.3V, R _L =500Ω			4.3	ns

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

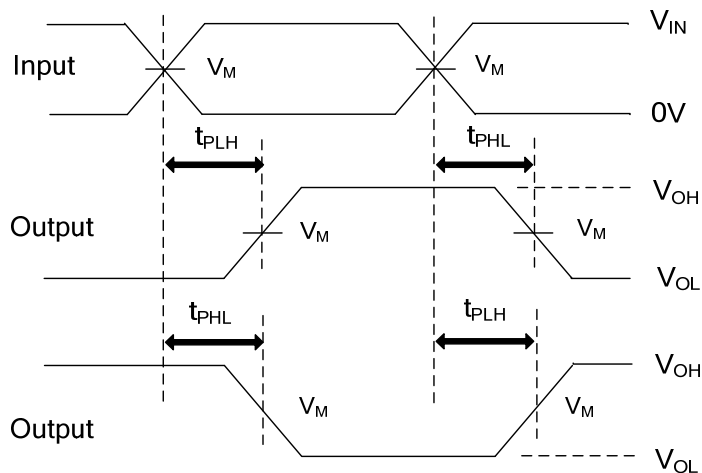
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C _{PD}	V _{CC} =3.3V±0.3V, C _L =50pF, f=10MHz		9.5		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

V_{CC}	INPUTS		V_M	C_L	R_L
	V_{IN}	t_R / t_F			
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	30pF	1K Ω
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	30pF	500 Ω
2.7V	2.7V	$\leq 2.5ns$	1.5V	50pF	500 Ω
$3.3V \pm 0.3V$	2.7V	$\leq 2.5ns$	1.5V	50pF	500 Ω



PROPAGATION DELAY TIMES

Note: C_L includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: PRR $\leq 10MHz$, $Z_o = 50\Omega$.

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