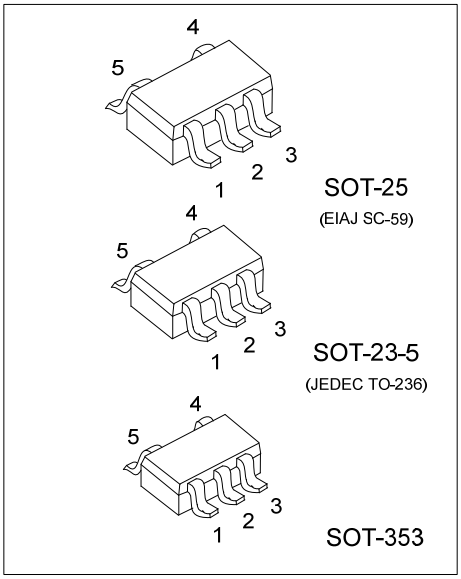
SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP



■ DESCRIPTION

The **U74LVC1G80** is a single positive-edge-triggered D-type flip-flop is designed for 1.65V to 5.5V V_{CC} operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the $\overline{Q}$ output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the level at the output.

This device is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

■ FEATURES

* Operate from 1.65V to 5.5V
* Inputs accept voltages to 5.5V
* I_{OFF} supports partial-power-down mode
* Low power dissipation: I_{CC}=10μA (Max.)
* ±24mA output drive (V_{CC}=3.3V)

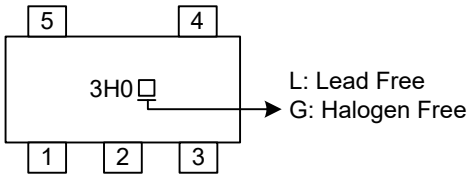
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC1G80L-AE5-R	U74LVC1G80G-AE5-R	SOT-23-5	Tape Reel
U74LVC1G80L-AF5-R	U74LVC1G80G-AF5-R	SOT-25	Tape Reel
U74LVC1G80L-AL5-R	U74LVC1G80G-AL5-R	SOT-353	Tape Reel

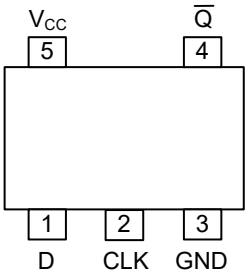
U74LVC1G80G-AE5-R
(1)Packing Type
(2) Package Type
(3) Green Package

(1) R: Tape Reel
(2) AE5: SOT-23-5, AF5: SOT-25, AL5: SOT-353
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION



■ PIN DESCRIPTION

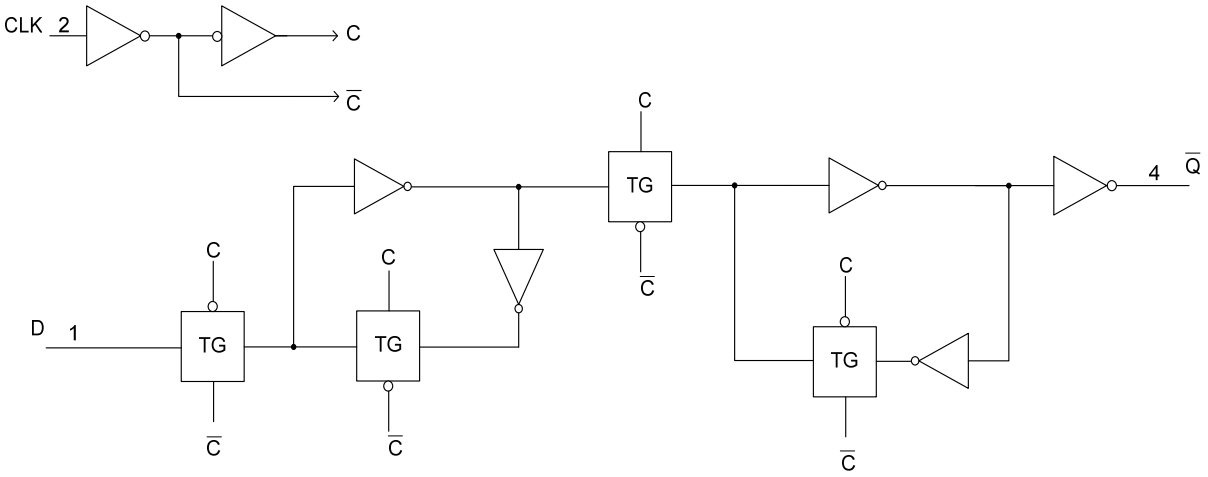
PIN NO.	PIN NAME	I/O	DESCRIPTION
1	D	I	Data Input
2	CLK	I	Clocking Input
3	GND		Ground Pin
4	$\overline{Q}$	O	Flip-Flop Output
5	V_{CC}		Power Pin

■ FUNCTION TABLE (EACH GATE)

INPUT		OUTPUT
CLK	D	$\overline{Q}$
↑	H	L
↑	L	H
L	X	Q_0

Note: H: HIGH voltage level; L: LOW voltage level; X: Don't care; ↑: Low to High CLK transition
Q_0: indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CLK transition

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		V_{CC}	-0.5 ~ +6.5	V
Input Voltage		V_{IN}	-0.5 ~ +6.5	V
Output Voltage	Output in the high or low state	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
	Output in the high-impedance or power-off state		-0.5 ~ +6.5	V
V_{CC} or GND Current		I_{CC}	±100	mA
Continuous Output Current		I_{OUT}	±50	mA
Continuous Current Through V_{CC} or GND)			±100	mA
Input Clamp Current (V_{IN}<0)		I_{IK}	-50	mA
Output Clamp Current (V_{OUT}<0)		I_{OK}	-50	mA
Storage Temperature Range		T_{STG}	-65 ~ +150	°C
Operating Temperature		T_A	-40 ~ +125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
High-Level Input Voltage	V_{IH}	V_{CC}=1.65V~1.95V	0.65xV_{CC}			V
		V_{CC}=2.3V~2.7V	1.7			V
		V_{CC}=3.0V~3.6V	2			V
		V_{CC}=4.5V~5.5V	0.7xV_{CC}			V
Low-Level Input Voltage	V_{IL}	V_{CC}=1.65V~1.95V			0.35xV_{CC}	V
		V_{CC}=2.3V~2.7V			0.7	V
		V_{CC}=3.0V~3.6V			0.8	V
		V_{CC}=4.5V~5.5V			0.3xV_{CC}	V
High-level Output Current	I_{OH}	V_{CC}=1.65V			-4	mA
		V_{CC}=2.3V			-8	mA
		V_{CC}=3.0V			-16	mA
					-24	mA
		V_{CC}=4.5V			-32	mA
Low-level Output Current	I_{OL}	V_{CC}=1.65V			4	mA
		V_{CC}=2.3V			8	mA
		V_{CC}=3.0V			16	mA
					24	mA
		V_{CC}=4.5V			32	mA
Input Transition Rise or Fall Rate	Δt/Δv	V_{CC}=1.8V±0.15V, 2.5V±0.2V			20	ns/V
		V_{CC}=3.3V±0.3V			10	ns/V
		V_{CC}=5 V±0.5V			5	ns/V

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	V_{CC}=1.65V~5.5V, I_{OH}=-100μA	V_{CC}-0.1			V
		V_{CC}=1.65V, I_{OH}=-4mA	1.2			V
		V_{CC}=2.3V, I_{OH}=-8mA	1.9			V
		V_{CC}=3.0V, I_{OH}=-16mA	2.4			V
		V_{CC}=3.0V, I_{OH}=-24mA	2.3			V
		V_{CC}=4.5V, I_{OH}=-32mA	3.8			V
Low-Level Output Voltage	V_{OL}	V_{CC}=1.65V~5.5V, I_{OL}=-100μA			0.1	V
		V_{CC}=1.65V, I_{OL}=4mA			0.45	V
		V_{CC}=2.3V, I_{OL}=8mA			0.3	V
		V_{CC}=3.0V, I_{OL}=16mA			0.4	V
		V_{CC}=3.0V, I_{OL}=24mA			0.55	V
		V_{CC}=4.5V, I_{OL}=32mA			0.55	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=0V~5.5V, V_{IN}=5.5V or GND			±10	μA
Power OFF Leakage Current	I_{OFF}	V_{CC}=0V, V_{IN} or V_{OUT}=5.5V			±10	μA
Quiescent Supply Current	I_Q	V_{CC}=1.65V ~ 5.5V, V_{IN}=5.5V or GND, I_{OUT}=0			10	μA
Additional Quiescent Supply Current	ΔI_Q	V_{CC} =3V~5.5V, One input at V_{CC}-0.6V, other inputs at V_{CC} or GND			500	μA
Input Capacitance	C_{IN}	V_{CC}=3.3V, V_{IN}=V_{CC} or GND		3.5		pF

■ DYNAMIC CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	Conditions		MIN	TYP	MAX	UNIT
Clock Frequency	f_{CLOCK}					160	MHZ
Pulse Duration, CLK High or Low	t_w	V_{CC}=1.8V±0.15V		2.5			ns
		V_{CC}=2.5V±0.2V		2.5			ns
		V_{CC}=3.3V±0.3V		2.5			ns
		V_{CC}=5V±0.5V		2.5			ns
Setup Time Before CLK ↑	t_{su}	V_{CC}=1.8V±0.15V	Data in high	2.3			ns
		V_{CC}=2.5V±0.2V		1.5			ns
		V_{CC}=3.3V±0.3V		1.3			ns
		V_{CC}=5V±0.5V		1.1			ns
		V_{CC}=1.8V±0.15V	Data in low	2.5			ns
		V_{CC}=2.5V±0.2V		1.5			ns
		V_{CC}=3.3V±0.3V		1.3			ns
		V_{CC}=5V±0.5V		1.1			ns
Hold Time, Data After CLK ↑	t_h	V_{CC}=1.8V±0.15V		0			ns
		V_{CC}=2.5V±0.2V		0.2			ns
		V_{CC}=3.3V±0.3V		0.9			ns
		V_{CC}=5V±0.5V		0.4			ns

■ SWITCHING CHARACTERISTIC (T_A=25°C, Input: t_R, t_F≤2.5ns; PRR≤1MHz)

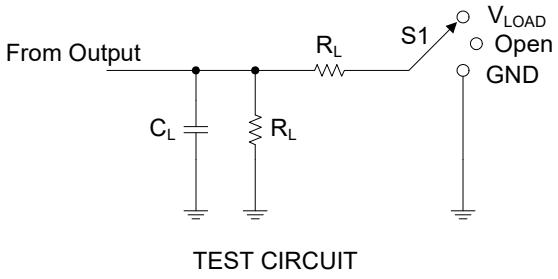
See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Maximum Clock Pulse Frequency	f_{MAX}	V_{CC} =1.65V~5.5V		160			MHz
Propagation Delay From Input (CLK) to Output ($\overline{Q}$)	t_{PLH}/t_{PHL}	V_{CC}=1.8V±0.15V	C_L=15pF	1.0		12.0	ns
		V_{CC}=2.5V±0.2V		1.0		9.0	ns
		V_{CC}=3.3V±0.3V		1.0		8.0	ns
		V_{CC}=5V±0.5V		1.0		6.5	ns
Propagation delay from input (CLK) to output($\overline{Q}$)	t_{PLH}/t_{PHL}	V_{CC}=1.8V±0.15V	C_L=30pF or 50pF	1.0		14.5	ns
		V_{CC}=2.5V±0.2V		1.0		10.5	ns
		V_{CC}=3.3V±0.3V		1.0		8.0	ns
		V_{CC}=5V±0.5V		1.0		7.5	ns

■ OPERATING CHARACTERISTICS (f=10MHz, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	V_{CC}=1.8V		24		pF
		V_{CC}=2.5V		24		pF
		V_{CC}=3.3V		25		pF
		V_{CC}=5V		27		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT

TEST	S1
t_{PLH} / t_{PHL}	OPEN
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZL}	GND

Fig.1 Load circuitry for switching times.

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_{IN}	t_r, t_f					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2×V_{CC}	15pF	1MΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2×V_{CC}	15pF	1MΩ	0.15V
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	15pF	1MΩ	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	2×V_{CC}	15pF	1MΩ	0.3V
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2×V_{CC}	30pF	1KΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2×V_{CC}	30pF	500Ω	0.15V
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	2×V_{CC}	50pF	500Ω	0.3V

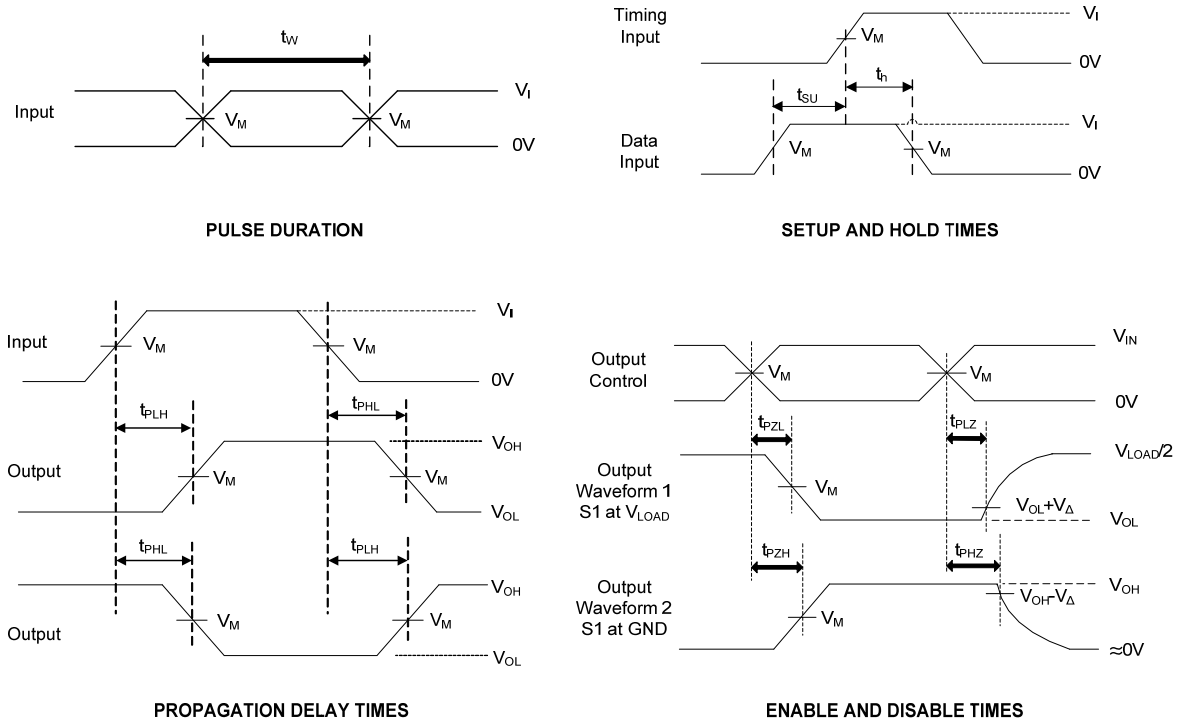


Fig. 2 Propagation delay from input to output and input voltage waveforms.

■ TEST CIRCUIT AND WAVEFORMS (Cont)

Notes: 1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control
3. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z = 50 Ω, slew rate 1 V/ns.
4. The outputs are measured one at a time, with one transition per measurement.
5. t_{PLH} and t_{PHZ} are the same as t_{dis}.
6. t_{PZL} and t_{PZH} are the same as t_{en}.
7.t_{PLH} and t_{PHL} are the same as t_{PD}.
8. All parameters and waveforms are not applicable to all devices.