



U74AUC1G125

Preliminary

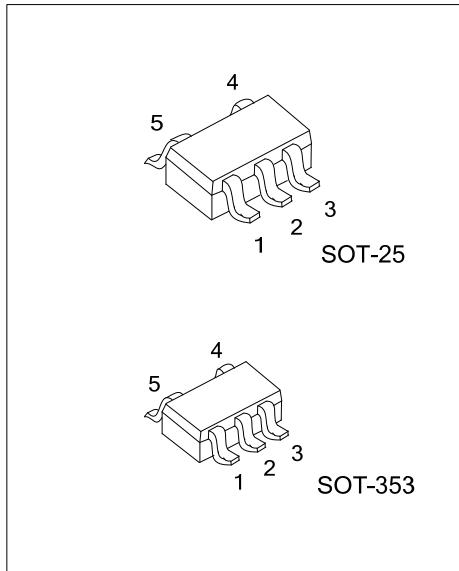
CMOS IC

SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

■ DESCRIPTION

The **U74AUC1G125** is a single line driver with a 3-state output. The output is disabled when the output-enable (\overline{OE}) input is high.

The AUC logic family is specifically designed for speed and is optimized for operation between 1.65V and 1.95V V_{CC} . With an optimal supply and 15pF load the device can operate at over 250 MHz, or 500 Mbps. The unique output structure of the AUC family provides great signal integrity without the need for external termination when driving 50- to 65Ω transmission lines of moderate length (less than 15 cm).



■ FEATURES

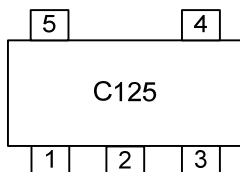
- * Operate from 0.9V to 2.7V
- * Low power dissipation: $I_{CC}=10\mu A$ (Max.)
- * $\pm 8mA$ Output Driver : $V_{CC}=1.8V$
- * I_{OFF} Supports partial-Power-Down Mode Operation and back drive protection

■ ORDERING INFORMATION

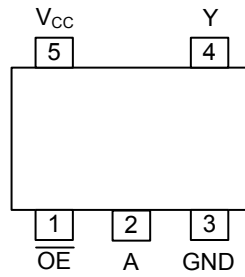
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AUC1G125L-AF5-R	U74AUC1G125G-AF5-R	SOT-25	Tape Reel
U74AUC1G125L-AL5-R	U74AUC1G125G-AL5-R	SOT-353	Tape Reel

<p>U74AUC1G125G-AF5-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) AF5: SOT-25, AL5: SOT-353 (3) G: Halogen Free and Lead Free</p>
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■ MARKING



■ PIN CONFIGURATION

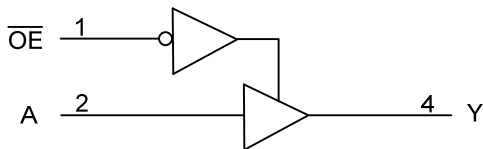


■ FUNCTION TABLE

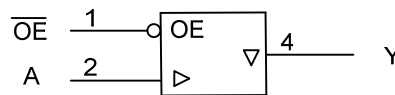
INPUT(\overline{OE})	INPUT(A)	OUTPUT(Y)
L	H	H
L	L	L
H	X	Z

Note: H: HIGH voltage level; L: LOW voltage level; X=don't care; Z=high-impedance OFF-state.

■ LOGIC DIAGRAM (positive logic)



Logic Symbol



IEC Logic Symbol

■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +3.6	V
Input Voltage	V_{IN}		-0.5 ~ +3.6	V
Output Voltage	V_{OUT}	Enable mode	-0.5 ~ $V_{CC} + 0.5$	V
		Power-down mode	-0.5 ~ +3.6	V
V_{CC} or GND Current	I_{CC}		±100	mA
Continuous Output Current	I_{OUT}	$V_{OUT}=0 \sim V_{CC}$	±20	mA
Input Clamp Current	I_{IK}	$V_{IN}<0$	-50	mA
Output Clamp Current	I_{OK}	$V_{OUT}<0$	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	0.9		2.7	V
Input Voltage	V_{IN}		0		3.6	V
Output Voltage	V_{OUT}	High or low state	0		V_{CC}	V
Operating Temperature	T_A		-40		+125	°C
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC}=0.8V \sim 1.6V$			20	ns/V
		$V_{CC}=1.65V \sim 1.95V$			10	ns/V
		$V_{CC}=2.3V \sim 2.7V$			3	ns/V

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25^\circ C$			$T_A=-40\sim+125^\circ C$			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-level Input Voltage	V_{IH}	$V_{CC}=0.9V$	V_{CC}			V_{CC}			V
		$V_{CC}=1.1V \sim 1.95V$	$0.65 \times V_{CC}$			$0.65 \times V_{CC}$			V
		$V_{CC}=2.3V \sim 2.7V$	1.7			1.7			V
Low-level Input Voltage	V_{IL}	$V_{CC}=0.9V$			0			0	V
		$V_{CC}=1.1V \sim 1.95V$			$0.35 \times V_{CC}$			$0.35 \times V_{CC}$	V
		$V_{CC}=2.3V \sim 2.7V$			0.7			0.7	V
High-Level Output Voltage	V_{OH}	$V_{CC}=0.9V \sim 2.7V, I_{OH}=-100\mu A$	$V_{CC}-0.1$			$V_{CC}-0.1$			V
		$V_{CC}=0.9V, I_{OH}=-0.7mA$		0.45			0.45		V
		$V_{CC}=1.1V, I_{OH}=-3mA$	0.8			0.6			V
		$V_{CC}=1.4V, I_{OH}=-5mA$	1			0.8			V
		$V_{CC}=1.65V, I_{OH}=-8mA$	1.2			1			V
Low-Level Output Voltage	V_{OL}	$V_{CC}=0.9V \sim 2.7V, I_{OL}=100\mu A$			0.2			0.2	V
		$V_{CC}=0.9V, I_{OL}=0.7mA$		0.25			0.35		V
		$V_{CC}=1.1V, I_{OL}=3mA$			0.3			0.4	V
		$V_{CC}=1.4V, I_{OL}=5mA$			0.4			0.5	V
		$V_{CC}=1.65V, I_{OL}=8mA$			0.45			0.6	V
		$V_{CC}=2.3V, I_{OL}=9mA$			0.6			0.8	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Leakage Current A or $\overline{\text{OE}}$ Input	I _{I(LEAK)}	V _{CC} =2.7V, V _{IN} = V _{CC} or GND			±5			±5	μA
Power OFF Leakage Current	I _{OFF}	V _{CC} =0V, V _{IN} or V _{OUT} =2.7V			±10			±10	μA
3-state Output OFF-state Current	I _{OZ}	V _{CC} =2.7V, V _{OUT} =V _{CC} or GND			±10			±10	μA
Quiescent Supply Current	I _{CC}	V _{CC} =0.9V to 2.7V, V _{IN} =V _{CC} or GND, I _{OUT} =0			10			10	μA

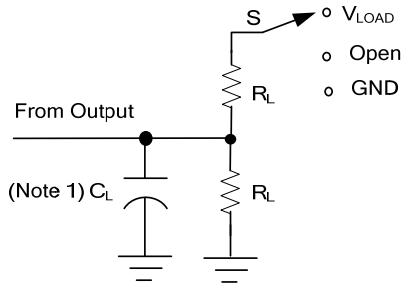
■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
Propagation Delay from Input (A) to Output (Y)	t _{PLH} / t _{PHL}	C _L =15pF, R _L =2kΩ	V _{CC} =0.9V		25		25		ns	
			V _{CC} =1.2±0.1V	6.1		10.5	5.5		12.5	ns
			V _{CC} =1.5±0.1V	4.5		8.5	3.5		10.5	ns
			V _{CC} =1.8±0.15V	2.5		5.5	1.5		7.5	ns
			V _{CC} =2.5±0.2V	1		3.1	0.5		5	ns
		C _L =30pF, R _L =1kΩ	V _{CC} =1.8±0.15V	2.5		5.5	1.8		7.5	ns
3-State Output Enable time from Input ($\overline{\text{OE}}$) to Output (Y)	t _{PZH} / t _{PZL}	C _L =15pF, R _L =2kΩ	V _{CC} =0.9V		25		25		ns	
			V _{CC} =1.2±0.1V	8.5		13	7.5		14.5	ns
			V _{CC} =1.5±0.1V	6		10	5.5		11.5	ns
			V _{CC} =1.8±0.15V	4		7	3.5		8.5	ns
			V _{CC} =2.5±0.2V	0.5		3.3	0.2		4.5	ns
		C _L =30pF, R _L =1kΩ	V _{CC} =1.8±0.15V	4.5		7.5	3.5		8.5	ns
3-State Output Disable time from Input ($\overline{\text{OE}}$) to Output (Y)	t _{PLZ} / t _{PLH}	C _L =15pF, R _L =2kΩ	V _{CC} =0.9V		25		25		ns	
			V _{CC} =1.2±0.1V	3.8		9.5	2.5		12.5	ns
			V _{CC} =1.5±0.1V	2.3		8.6	1.8		10.5	ns
			V _{CC} =1.8±0.15V	1.5		7.2	1		9.2	ns
			V _{CC} =2.5±0.2V	0.9		5	0.5		6.5	ns
		C _L =30pF, R _L =1kΩ	V _{CC} =1.8±0.15V	1.8		7.2	1.1		8.5	ns
3-State Output Disable time from Input ($\overline{\text{OE}}$) to Output (Y)	t _{PLZ} / t _{PLH}	C _L =30pF, R _L =500Ω	V _{CC} =2.5±0.2V	0.8		4	0.4		5.5	ns

■ OPERATING CHARACTERISTICS (f=10MHz, T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C _I	V _{CC} =2.5V, V _{IN} =V _{CC} or GND		5		pF
Output Capacitance	C _O	V _{CC} =2.5V, V _{IN} =V _{CC} or GND		7.6		pF
Power Dissipation Capacitance (Outputs enabled)	C _{PD}	V _{CC} =0.9V		14		pF
		V _{CC} =1.2V		14		pF
		V _{CC} =1.5V		14		pF
		V _{CC} =1.8V		15		pF
		V _{CC} =2.5V		16		pF
Power Dissipation Capacitance (Outputs Disabled)	C _{PD}	V _{CC} =0.9V		1.5		pF
		V _{CC} =1.2V		1.5		pF
		V _{CC} =1.5V		1.5		pF
		V _{CC} =1.8V		2		pF
		V _{CC} =2.5V		2.5		pF

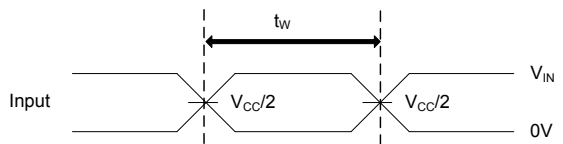
TEST CIRCUIT AND WAVEFORMS



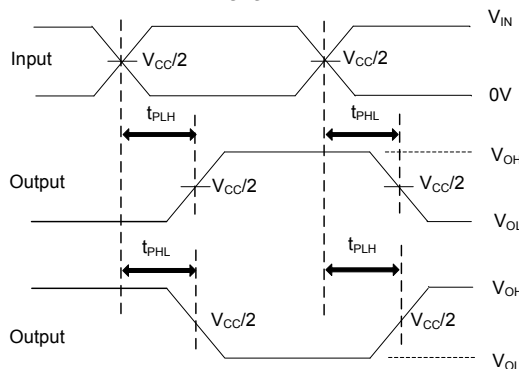
TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$

TEST CIRCUIT

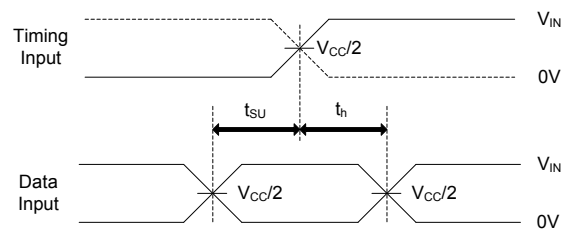
V_{CC}	C_L	R_L	V_{Δ}
0.9V	15pF	2k Ω	0.1V
1.2V \pm 0.1V	15pF	2k Ω	0.1V
1.5V \pm 0.1V	15pF	2k Ω	0.1V
1.8V \pm 0.15V	15pF	2k Ω	0.15V
2.5V \pm 0.2V	15pF	2k Ω	0.15V
1.8V \pm 0.15V	30pF	1k Ω	0.15V
2.5V \pm 0.2V	30pF	500 Ω	0.15V



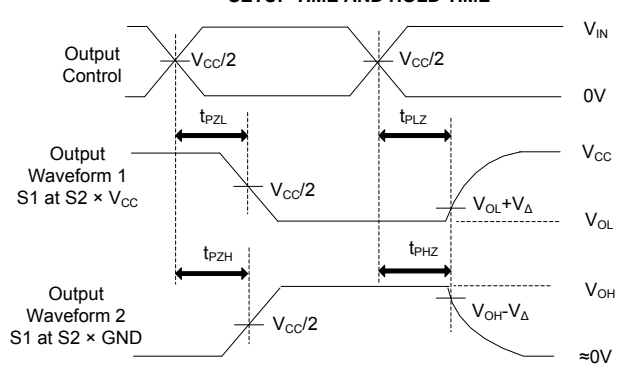
PULSE WIDTH



PROPAGATION DELAY TIMES



SETUP TIME AND HOLD TIME



ENABLE AND DISABLE TIMES

■ TEST CIRCUIT AND WAVEFORMS (Cont.)

Notes: 1. C_L includes probe and jig capacitance.

2. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control

3. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, $Z = 50 \Omega$, slew rate 1 V/ns.

4. The outputs are measured one at a time, with one transition per measurement.

5. t_{PLH} and t_{PHZ} are the same as t_{dis} .

6. t_{PZL} and t_{PZH} are the same as t_{en} .

7. t_{PLH} and t_{PHL} are the same as t_{PD}

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