

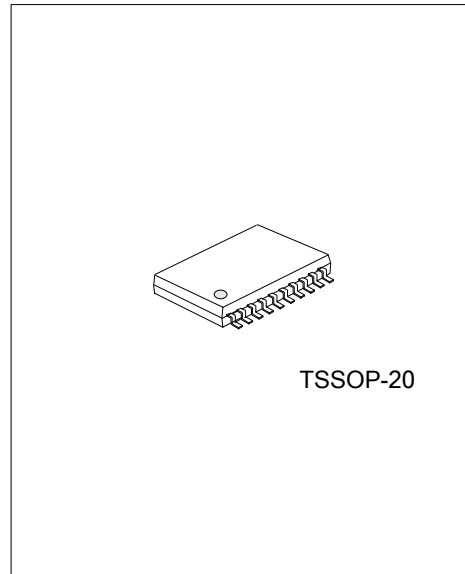


U74CB3Q3244

Advance

CMOS IC

8-BIT FET BUS SWITCH 2.5V/3.3V LOW-VOLTAGE HIGH-BANDWIDTH BUS SWITCH



DESCRIPTION

The **U74CB3Q3244** is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance.

The **U74CB3Q3244** is organized as two 4-bit bus switches with separate output-enable ($\overline{OE1}$ or $\overline{OE2}$) input, It can be used as two 4-bit bus switches or as one 8-bit bus switch.

This device is fully specified for partial-power-down applications using I_{OFF} . The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FEATURES

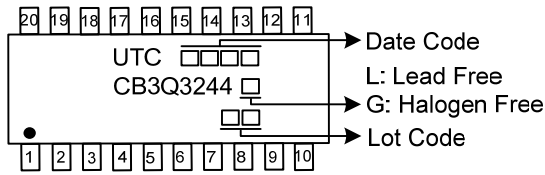
- * Data and control inputs provide undershoot clamp diodes
- * Operating voltage range of 2.3V to 3.6V
- * Control inputs can be driven by TTL or 5V/3.3V CMOS outputs
- * Low power consumption I_{CC} : 0.7mA (Typ.)
- * Data I/O support 0 to 5V signaling levels (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V)
- * I_{OFF} supports live insertion, partial-power-down mode, back-drive protection

ORDERING INFORMATION

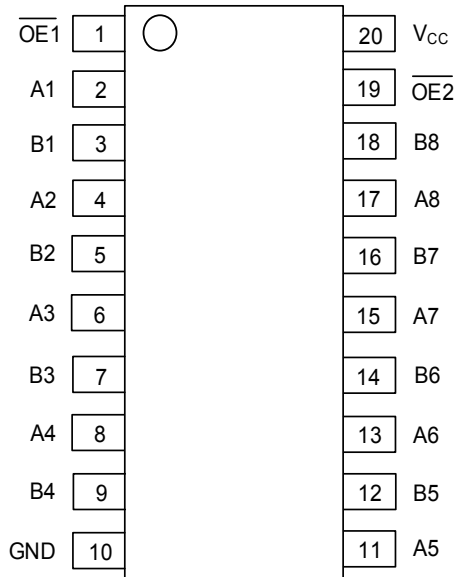
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CB3Q3244L-P20-R	U74CB3Q3244G-P20-R	TSSOP-20	Tape Reel

<p>U74CB3Q3244G-P20-R</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) R: Tape Reel (2) P20: TSSOP-20 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



PIN CONFIGURATION

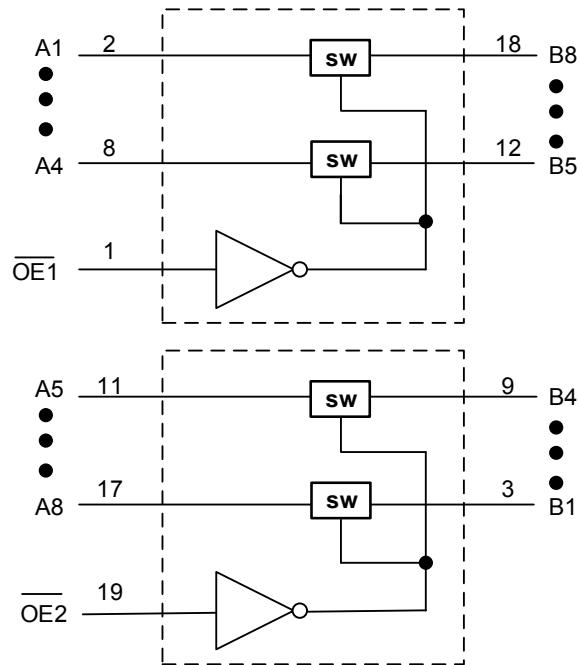


FUNCTION TABLE

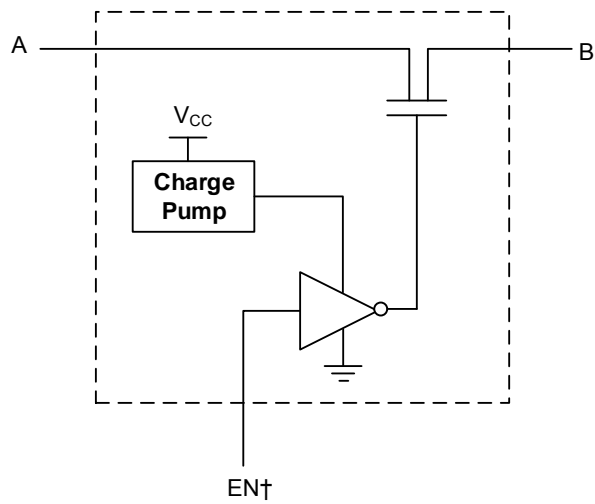
INPUTS(\overline{OE})	INPUTS/OUTPUTS(A)
L	B
H	Z

Note: H: HIGH Voltage Level, L: LOW Voltage Level, Z: High Impedance, X: Don' Care

■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 4.6	V
Input Voltage	V_{IN}	-0.5 ~ 7	V
V_{CC} or GND Current	I_{CC}	±100	mA
Output Current	I_{OUT}	±64	mA
Input Clamp Current	I_{IK}	±50	mA
Output Clamp Current	I_{OK}	±50	mA
Storage Temperature	T_{STG}	-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	83	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.3		3.6	V
High-level Input Voltage	V_{IH}	$V_{CC}=2.3V\sim 2.7V$	1.7		5.5	V
		$V_{CC}=2.7V\sim 3.6V$	2		5.5	V
Low-level Input Voltage	V_{IL}	$V_{CC}=2.3V\sim 2.7V$	0		0.7	V
		$V_{CC}=2.7V\sim 3.6V$	0		0.8	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Temperature	T_A		-40		+125	°C

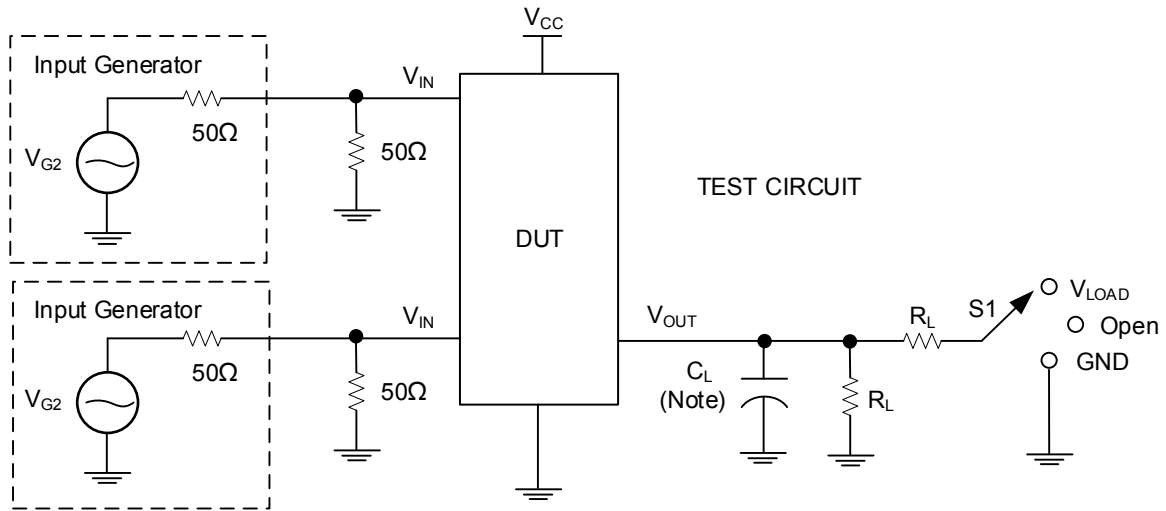
■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=3.6V$, $V_{IN}=V_{CC}$ or GND			±1	μA	
3-state Output Off-state Current	I_{OZ}	$V_{CC}=3.6V$, $V_{OUT}=V_{CC}$ or GND, $V_I=V_{IH}$ or V_{IL} , $I_{OUT}=0$			±1	μA	
Quiescent Supply Current	I_{CC}	$V_{CC}=3.6V$, $V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$		0.7	2	mA	
Additional Quiescent Device Current Per Input Pin	ΔI_{CC}	$V_{CC}=3.6V$, One input at 3V, Other inputs at 0 or V_{CC}			30	μA	
Input Capacitance	C_I	$V_{CC}=3.3V$, $V_{IN}=5.5V, 3.3V$ or GND		2.5	3.5	pF	
"ON" Resistance	R_{ON}	$V_{CC}=2.3V$, TYP at $V_{CC}=2.5V$	$V_I=0V$, $I_{OUT}=30mA$		4	8	Ω
			$V_I=1.7V$, $I_{OUT}=-15mA$		5	9	Ω
		$V_{CC}=3V$	$V_I=0V$, $I_{OUT}=30mA$		4	6	Ω
			$V_I=2.4V$, $I_{OUT}=-15mA$		5	8	Ω

■ SWITCHING CHARACTERISTICS ($C_L=50pF$, $T_A=25^\circ\text{C}$, unless otherwise specified)

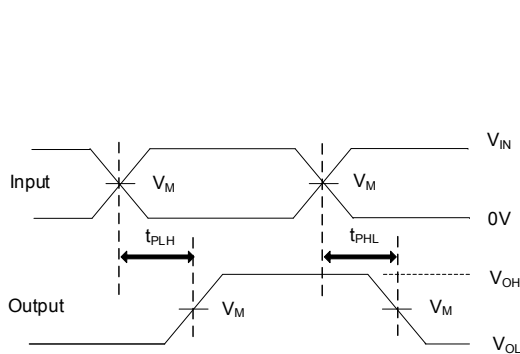
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from Input (A or B) to Output (B or A)	t_{PD}	$V_{CC}=2.5V\pm 0.2V$			0.12	ns
		$V_{CC}=3.3V\pm 0.3V$			0.2	
Enable Delay Time, Input \overline{OE} to Output (A or B)	t_{EN}	$V_{CC}=2.5V\pm 0.2V$	2.8		7.1	ns
		$V_{CC}=3.3V\pm 0.3V$	2.5		5.9	
Disable Delay Time, Input \overline{OE} to Output (A or B)	t_{DIS}	$V_{CC}=2.5V\pm 0.2V$	1		5.8	ns
		$V_{CC}=3.3V\pm 0.3V$	1.5		5.8	

■ TEST CIRCUIT AND WAVEFORMS

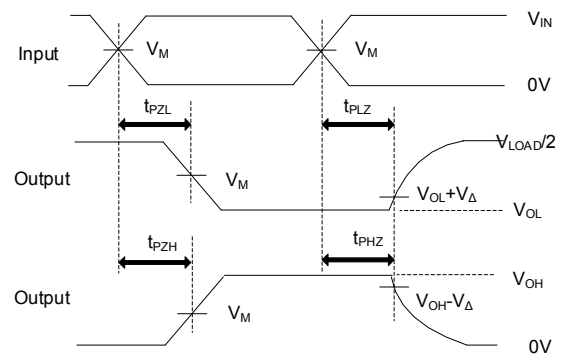


Note: C_L includes probe and jig capacitance.

V _{CC}	S1	R _L	V _{IN}	C _L	V _Δ
2.5V±0.2V	Open	500Ω	V _{CC} or GND	30pF	
3.3V±0.3V	Open	500Ω	V _{CC} or GND	50pF	
2.5V±0.2V	2×V _{CC}	500Ω	GND	30pF	0.15V
3.3V±0.3V	2×V _{CC}	500Ω	GND	50pF	0.3V
2.5V±0.2V	GND	500Ω	V _{CC}	30pF	0.15V
3.3V±0.3V	GND	500Ω	V _{CC}	50pF	0.3V



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

- Notes: 1. C_L includes probe and test-fixture capacitance
 2. All input pulses are supplied by generators having the following characteristics: PRR ≤1MHz, Z_o= 50Ω, t_r=6ns, t_f=6ns

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