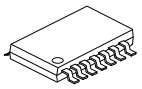
QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS



TSSOP-14

■ DESCRIPTION

The **U74AUC125** device is designed for 0.8V to 2.7V V_{CC} operation, but is designed specifically for 1.6V to 1.95V V_{CC} operation.

This device contains four independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable input is high. To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

■ FEATURES

* Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
* I_{OFF} supports live insertion, partial-power-down mode, back-drive protection
* Inputs accept voltages up to 2.7V
* Max t_{pd} of 2.1ns at 1.8V
* Low static power consumption; I_{CC}=±10μA (Max.)
* ±8mA Output Drive at 1.8V

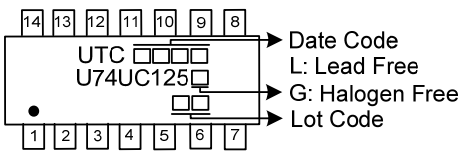
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74UC125L-P14-R	U74UC125G-P14-R	TSSOP-14	Tape Reel

U74UC125G-P14-R

(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) P14: TSSOP-14
(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



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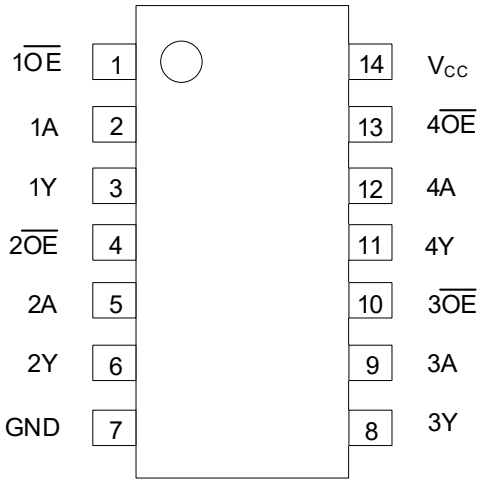
■ PIN CONFIGURATION

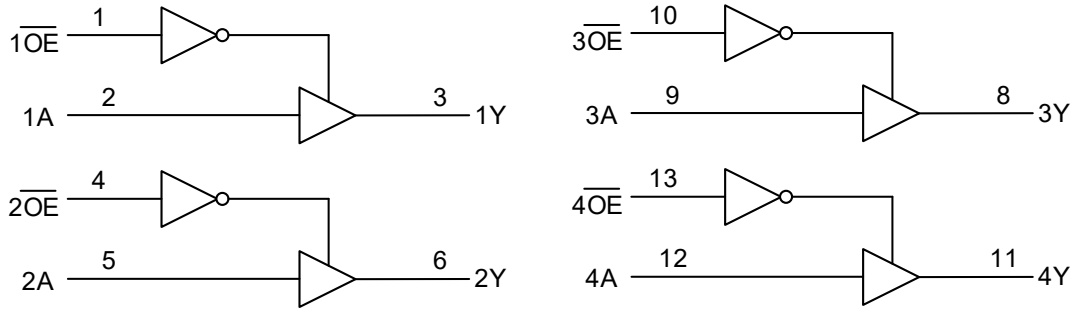


■ FUNCTION TABLE (each gate)

INPUT($\overline{OE}$)	INPUT(B)	OUTPUT(Y)
L	H	H
L	L	L
H	X	Z

Note: H: HIGH Voltage Level L: LOW Voltage Level Z: High Impedance X: Don' Care

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +3.6	V
Input Voltage	V_{IN}		-0.5 ~ +3.6	V
Output Voltage	V_{OUT}	Output in the high or low state	-0.5 ~ V_{CC} +0.5	V
		Output in the power-off state	-0.5 ~ +3.6	V
Continuous V_{CC} or GND Current	I_{CC}		±100	mA
Continuous Output Current	I_{OUT}		±50	mA
Input Clamp Current	I_{IK}	V_{IN}<0V	-50	mA
Output Clamp Current	I_{OK}	V_{OUT}<0V	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	0.8		2.7	V
Input Voltage	V_{IN}		0		3.6	V
Output Voltage	V_{OUT}	Active state	0		V_{CC}	V
		3-state	0		3.6	V
Input Transition Rise or Fall Rate	Δt/Δv				20	ns/V
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	V_{CC}= 0.8V	V_{CC}			V
		V_{CC}=1.1 ~ 1.95V	0.65× V_{CC}			V
		V_{CC}=2.3 ~ 2.7V	1.7			V
Low-Level Input Voltage	V_{IL}	V_{CC}= 0.8V			0	V
		V_{CC}=1.1 ~ 1.95V			0.35× V_{CC}	V
		V_{CC}=2.3 ~ 2.7V			0.7	V
High-Level Output Voltage	V_{OH}	V_{CC}=0.8 ~ 2.7V, I_{OH}=-100μA	V_{CC}-0.1			V
		V_{CC}=0.8V, I_{OH}=-0.7mA		0.46		V
		V_{CC}=1.1V, I_{OH}=-3mA	0.77			V
		V_{CC}=1.4V, I_{OH}=-5mA	1			V
		V_{CC}=1.65V, I_{OH}=-8mA	1.2			V
		V_{CC}=2.3V, I_{OH}=-9mA	1.8			V
Low-Level Output Voltage	V_{OL}	V_{CC}=0.8 ~ 2.7V, I_{OL}=100μA			0.2	V
		V_{CC}=0.8V, I_{OL}=0.7mA		0.25		V
		V_{CC}=1.1V, I_{OL}=3mA			0.3	V
		V_{CC}=1.4V, I_{OL}=5mA			0.4	V
		V_{CC}=1.65V, I_{OL}=8mA			0.45	V
		V_{CC}=2.3V, I_{OL}=9mA			0.6	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}= 0 ~ 2.7V, V_{IN} = V_{CC} or GND			±5	μA
Power Off Leakage Current	I_{OFF}	V_{CC}=0V, V_{IN} or V_{OUT}=2.7V			±10	μA
Quiescent Supply Current	I_{CC}	V_{CC}=0.8 ~ 2.7V, V_{IN}= V_{CC} or GND, I_{OUT}=0			10	μA

Note: I_{OL} and I_{OH} are tested one output at a time.

■ SWITCHING CHARACTERISTICS

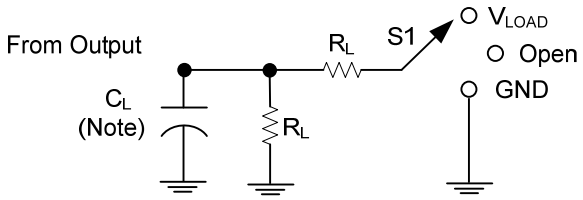
(T_A=25°C, Input: t_R=t_F=20ns, C_L=15pF, R_L=2KΩ, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from Input(A) to Output(Y)	t_{PD}	V_{CC}=0.8V±0.15V		5.8		ns
		V_{CC}=2.5V±0.2V	0.5		2.1	ns
Enable Delay Time, Input ($\overline{OE}$) to Output(Y)	t_{EN}	V_{CC}=0.8V±0.15V		7.5		ns
		V_{CC}=2.5V±0.2V	0.6		2.3	ns
Disable Delay Time, Input ($\overline{OE}$) to Output(Y)	t_{DIS}	V_{CC}=0.8V±0.15V		6.4		ns
		V_{CC}=2.5V±0.2V	0.8		2.3	ns

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Capacitance	C_{IN}	V_{CC}=2.5V, V_{IN}=V_{CC} or GND			2.5		pF
Output Capacitance	C_{OUT}	V_{CC}=2.5V, V_{OUT}=V_{CC} or GND			5		pF
Power Dissipation Capacitance	C_{PD}	Outputs enabled, f=10MHz	V_{CC}=0.8V,		15		pF
			V_{CC}=1.2V		15		pF
			V_{CC}=1.5V		15		pF
			V_{CC}=1.8V		16		pF
			V_{CC}=2.5V		17		pF
		Outputs disabled, f=10MHz	V_{CC}=0.8V,		2		pF
			V_{CC}=1.2V		2		pF
			V_{CC}=1.5V		2		pF
			V_{CC}=1.8V		3		pF
			V_{CC}=2.5V		4		pF

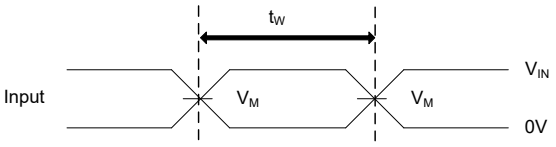
■ TEST CIRCUIT AND WAVEFORMS



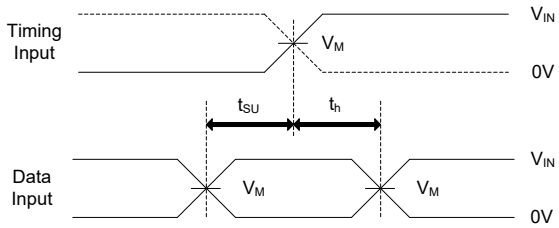
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

Note: C_L includes probe and jig capacitance.

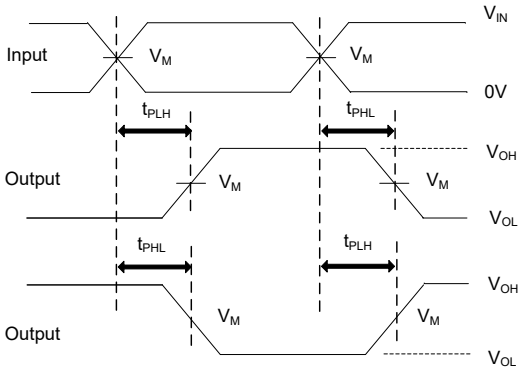
V_{CC}	C_L	R_L	V_Δ
.8V	15pF	2KΩ	0.1V
1.2V±0.1V	15pF	2KΩ	0.1V
1.5V±0.1V	15pF	2KΩ	0.1V
1.8V±0.15V	15pF	2KΩ	0.15V
2.5V±0.2V	15pF	2KΩ	0.15V
1.8V±0.15V	30pF	1KΩ	0.15V
2.5V±0.2V	30pF	500Ω	0.15V



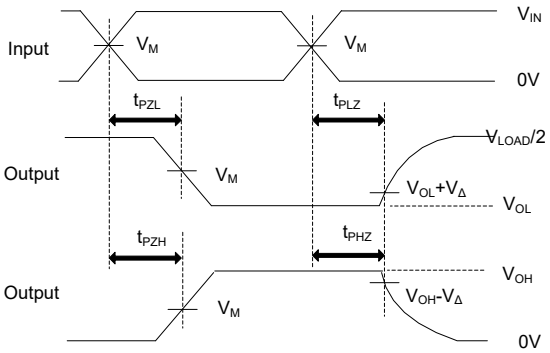
PULSE WIDTH



SETUP TIME AND HOLD TIME



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω.

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