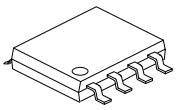
MICROPROCESSOR UP WATCH DOG TIMERE



SOP-8

■ DESCRIPTION

The UTC **UWD813** microprocessor supervisory circuit reduces the complexity and number of components required to monitor power-supply and monitor microprocessor activity. It significantly improves system reliability and accuracy compared to separate ICs or discrete components.

The UTC **UWD813** provides power-supply monitoring circuitry that generates a reset output during power-up, power-down and brownout conditions. The reset output remains operational with VCC as low as 1V. Independent watchdog monitoring circuitry is also provided. This is activated if the watchdog input has not been toggled within 1.9 seconds.

In addition, there is a 1.25V threshold detector for power-fail warning, low-battery detection, or monitoring an additional power supply. An active-low manual-reset input ($\overline{MR}$) is also included.

■ FEATURES

* Precision supply- Voltage Monitor
* Valid RESET remains with V_{CC} as low as 1V
* 200ms Reset Pulse Width
* Independent Watchdog Timer (1.9sec) Timeout
* Voltage Monitor for Power-Fail or Low-Battery Warning
* With Manual reset input

■ ORDERING INFORMATION

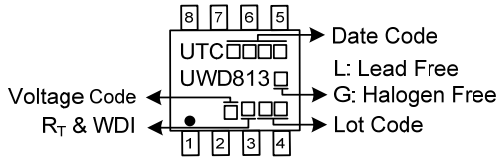
Ordering Number		Reset Time	Watch Dog Interval	UNIT	Code	Package	Packing
Lead Free	Halogen Free						
UWD813L-x-x-S08-R	UWD813G-x-x-S08-R	230	1761	ms	G	SOP-8	Tape Reel

Note: xx: Output Voltage.

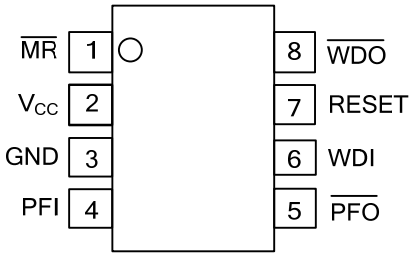
UWD817XG-x-x-S08-R

(1)Packing Type	(1) R: Tape Reel
(2)Package Type	(2) S08: SOP-8
(3)R_T & WDI	(3) refer to Reset Time & Watch Dog Interval
(4)Output Voltage Code	(4) x: Refer to Marking Information
(5)Green Package	(5) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING INFORMATION

PACKAGE	VOLTAGE CODE	MARKING
SOP-8	A : 2.63V B : 2.93V C : 3.08V D: 4.00V H: 4.40V G: 4.65V	

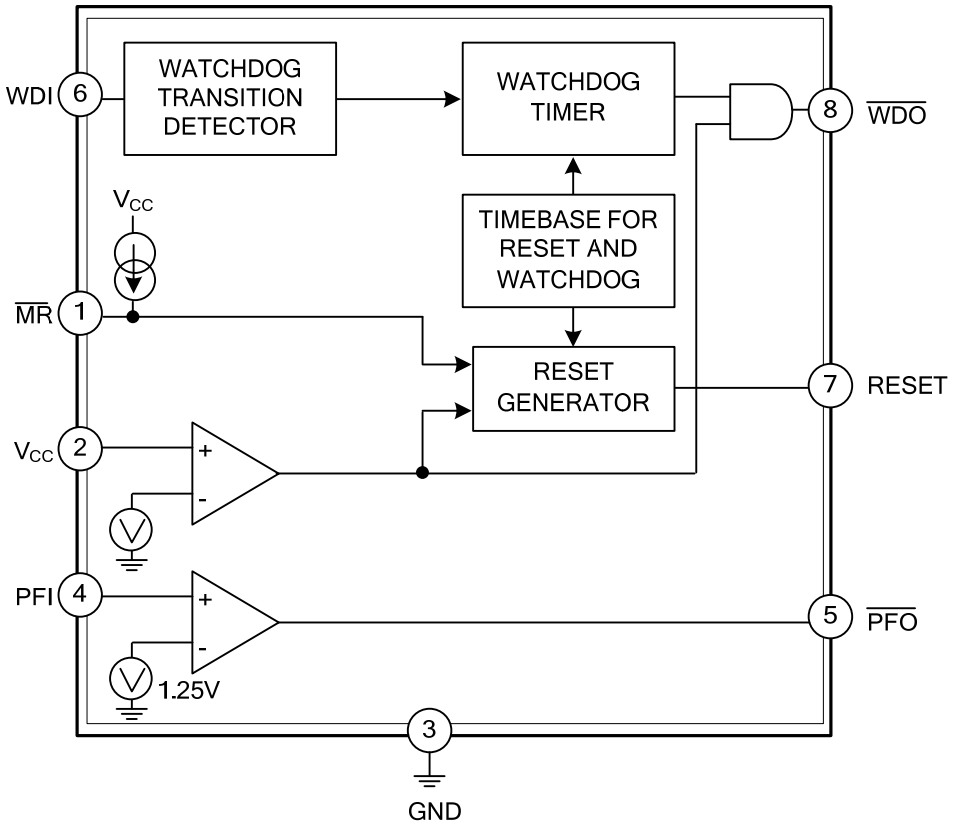
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	$\overline{MR}$	Manual-Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal 500μA (V_{CC}= +5V) pull-up current. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2	V_{CC}	Power Supply Voltage that is monitored.
3	GND	0V Ground Reference for all signals.
4	PFI	Power-Fail Voltage Monitor Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} when not used.
5	$\overline{PFO}$	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ stays high.
6	WDI	Watchdog Input. If WDI remains high or low for 1.9sec, the internal watchdog timer runs out and WDO goes low (BLOCK DIAGRAM). The internal watchdog timer clears whenever reset is asserted, when WDI sees a rising or falling edge.The Floating WDI buffer disables the watchdog feature.
7	RESET	Active-High Reset Output pulses high for 230ms when triggered, and stays high whenever V_{CC} is below the reset threshold. It remains high for 200ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout will not trigger RESET unless $\overline{WDO}$ is connected to $\overline{MR}$.
8	$\overline{WDO}$	Watchdog Output pulls low when the internal watchdog timer finishes its 1.9sec count and does not go high again until the watchdog is cleared. $\overline{WDO}$ also goes low during low-line conditions. Whenever V_{CC} is below the reset threshold, $\overline{WDO}$ stays low; however, unlike RESET, $\overline{WDO}$ does not have a minimum pulse width. As soon as V_{CC} rises above the reset threshold, $\overline{WDO}$ goes high with no delay.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Terminal Voltage (with respect to GND)	V_{CC}	-0.3 ~ 6.0	V
All Other Inputs	V_{IN}	-0.3 ~ (V_{CC}+0.3V)	V
Input Current, V_{CC}, GND	I_{CC}	20	mA
Output Current, (all outputs)	I_{OUT}	20	mA
Power Dissipation	PD	470	mW
Junction Temperature	T_J	+150	°C
Operating Temperature Range	T_{OPR}	-40 ~ +85	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (V_{CC}=4.75V ~ 5.5V, T_J=-40~+85°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		V_{CC}		1.0		5.5	V
Supply Current		I_{SUPPLY}	V_{CC}=5.5V		150	350	μA
Reset Threshold		V_{RT}		4.5	4.65	4.75	V
Reset Threshold Hysteresis					60		mV
Reset Pulse Width		t_{RS}	VCC to RESET	150	230	300	ms
Reset Output Voltage			VCC=1.2VI_{SOURCE} = 4μA	0.9			V
			VCC=4.5VI_{SOURCE} = 800μA	V_{CC}-1.5			V
			V_{CC}=5.5V, I_{sink}=3.2mA			0.4	V
Watchdog Timeout Period		t_{WD}		1	1.9	2.4	sec
WDI Pulse Width		t_{WP}	V_{IL}=0.4V V_{IH} = (V_{CC})(0.8)	50			ns
WDI Input Threshold	Low		V_{CC}=5V			0.8	V
	High		V_{CC}=5V	3.5			V
	Low		$V_{RST(MAX)}$< V_{CC}< 3.6V			0.5	V
	High		$V_{RST(MAX)}$< V_{CC}< 3.6V	0.7×V_{CC}			V
WDI Input Current			W_{DI}=V_{CC}		50	150	μA
			W_{DI}=0V	-150	-50		μA
$\overline{WDO}$ Output Voltage			VCC=5.5V, I_{SOURCE}=800μA	V_{CC}-1.5			V
			VCC=5.5V, I_{sink}=1.2mA			0.4	V
$\overline{MR}$ Pull-Up Current			$\overline{MR}$ = 0V	100	250	600	μA
$\overline{MR}$ Pulse Width		t_{MR}		150			ns
$\overline{MR}$ Input Threshold	Low		T_A = +25°C			0.8	V
	High			2			V
$\overline{MR}$ to Reset Out Delay		t_{MD}				350	ns
PFI Input Threshold				1.1	1.25	1.3	V
PFI Input Current			V_{CC}= 5V	-50	0.01	50	nA
$\overline{PFO}$ Output Voltage			I_{SOURCE}= 800μA	V_{CC}-1.5			V
			I_{sink}=3.2mA			0.4	V

■ APPLICATION NOTES

Ensuring a Valid RESET **Output Down to V_{CC}=0V**

When V_{CC} falls below 1V, the **UWD813** RESET output no longer sinks current—it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the RESET pin as shown in Figure 1, any stray charge or leakage currents will be drained to ground, holding RESET low. Resistor value (R1) is not critical. It should be about 100kΩ, large enough not to load RESET and small enough to pull RESET to ground.

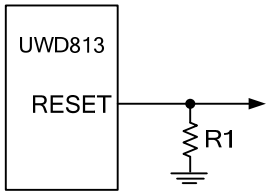


Figure 1. RESET Valid to Ground Circuit

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and $\overline{PFO}$. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. RESET can be asserted on other voltages in addition to the +5V V_{CC} line. Connect $\overline{PFO}$ to MR to initiate a RESET pulse when PFI drops below 1.25V. Figure 2 shows the **UWD813** configured to assert RESET when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

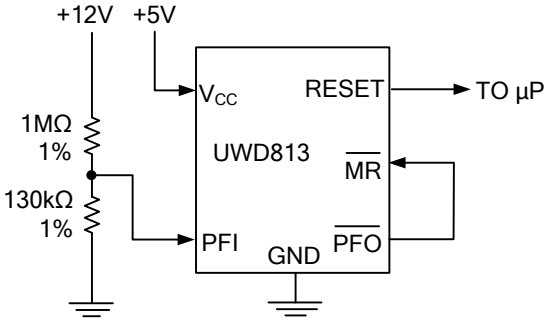
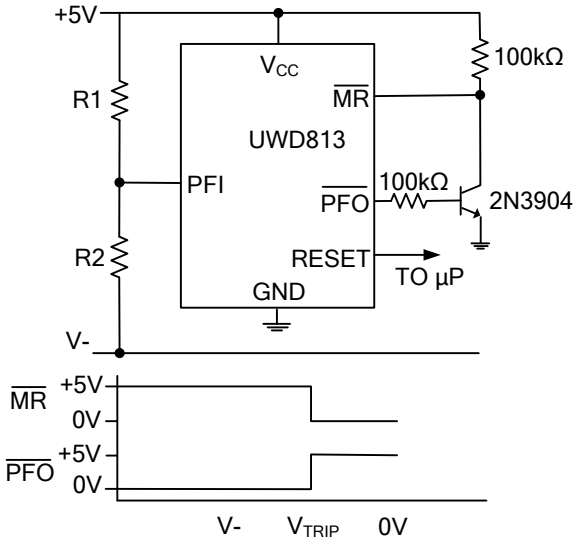


Figure 2.Monitoring Both +5V and +12V

■ APPLICATION NOTES (Cont.)

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 3). When the negative rail is good (a negative voltage of large magnitude), $\overline{PFO}$ is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), $\overline{PFO}$ is high. By adding the resistors and transistor as shown, a high $\overline{PFO}$ triggers reset. As long as $\overline{PFO}$ remains high, the **UWD813** will keep reset asserted (RESET = low, RESET = high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.



$$\frac{5-1.25}{R1}=\frac{1.25-V_{TRIP}}{R2} \qquad V_{TRIP}<0$$

Figure 3.Monitoring a Negative Voltage

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins can contend with the **UWD813** RESET output. If, for example, the RESET output is driven high and the Microprocessor wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the RESET output and the µP reset I/O, as in Figure 4. Buffer the RESET output to other system components.

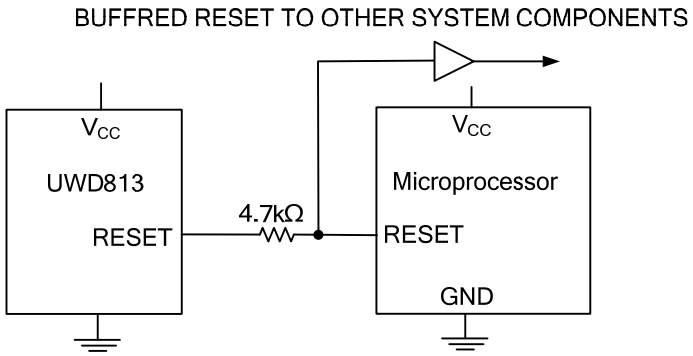
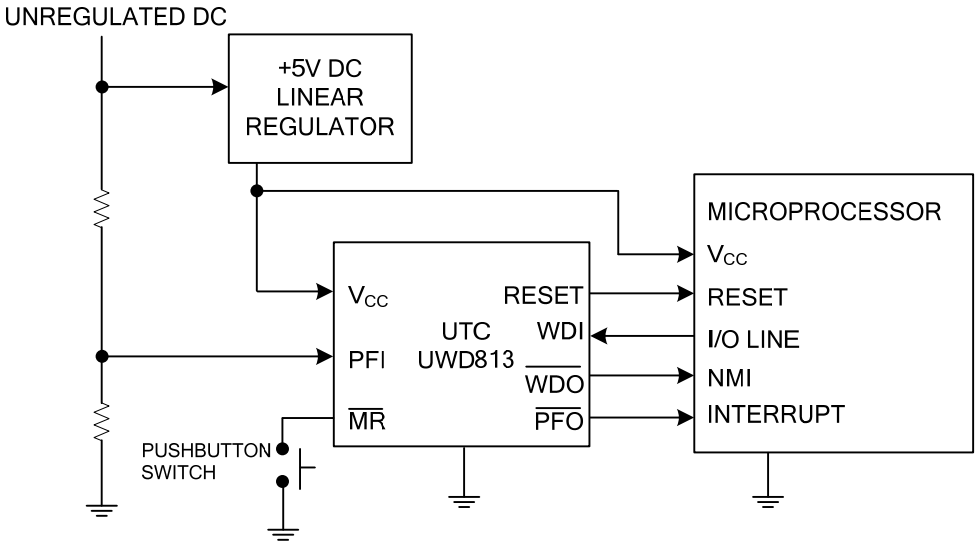


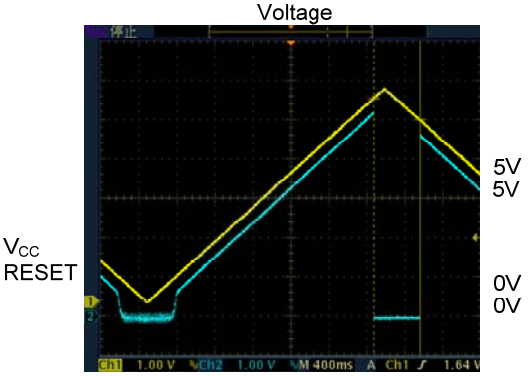
Figure 4. Interfacing to Microprocessors with Bidirectional Reset I/O

■ TYPICAL APPLICATION CIRCUIT



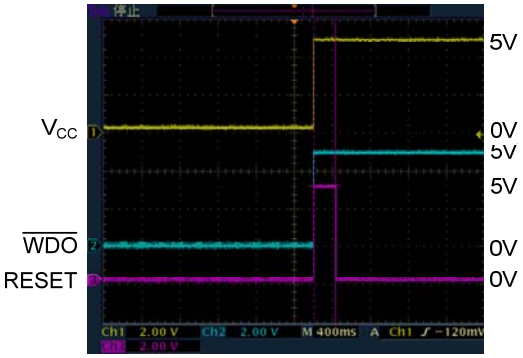
■ TYPICAL CHARACTERISTICS

Reset Output Voltage vs. Supply Voltage



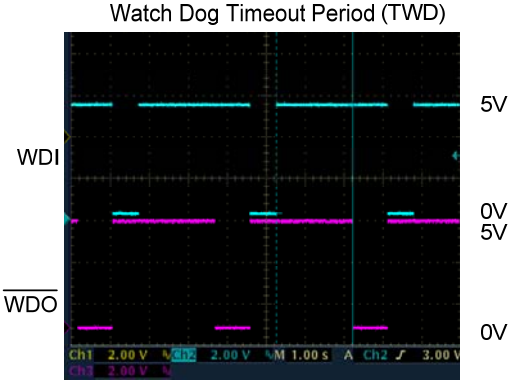
400mS/div

V_{CC} to Reset Delay Time



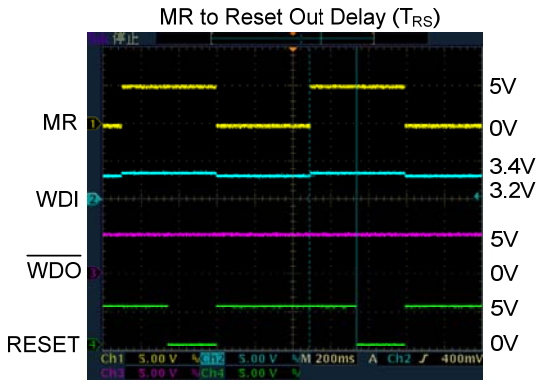
400mS/div

Watch Dog Timeout Period (TWD)



1S/div

MR to Reset Out Delay (T_{RS})



200mS/div