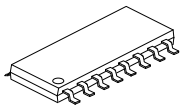
CMOS 4-BIT D-TYPE REGISTERS



SOP-16

■ DESCRIPTION

The UTC **UCD4076** are 4-bit registers consisting of D-type flip-flops that feature 3-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

■ FEATURES

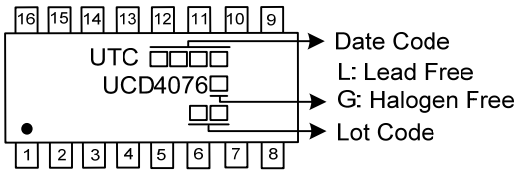
* Three-state outputs
* Input disabled without gating the clock
* Maximum input current of 1μA at 18V
  temperature range;100nA at 18V and 25°C
1V at V_{DD}=5V
  2V at V_{DD}=10V
  2.5V at V_{DD}=15V
* 5V,10V,and 15V parametric ratings

■ ORDERING INFORMATION

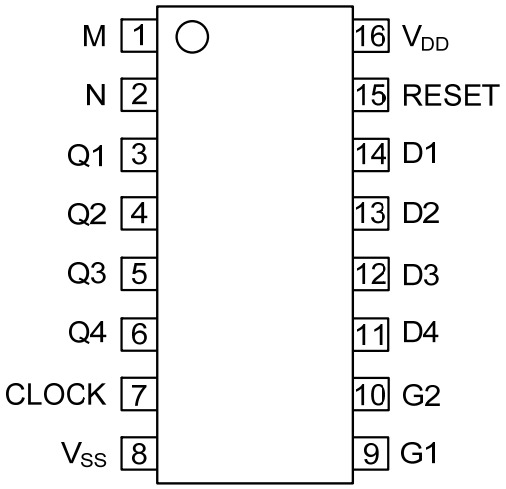
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCD4076L-S16-R	UCD4076G-S16-R	SOP-16	Tape Reel

UCD4076G-S16-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) S16: SOP-16 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

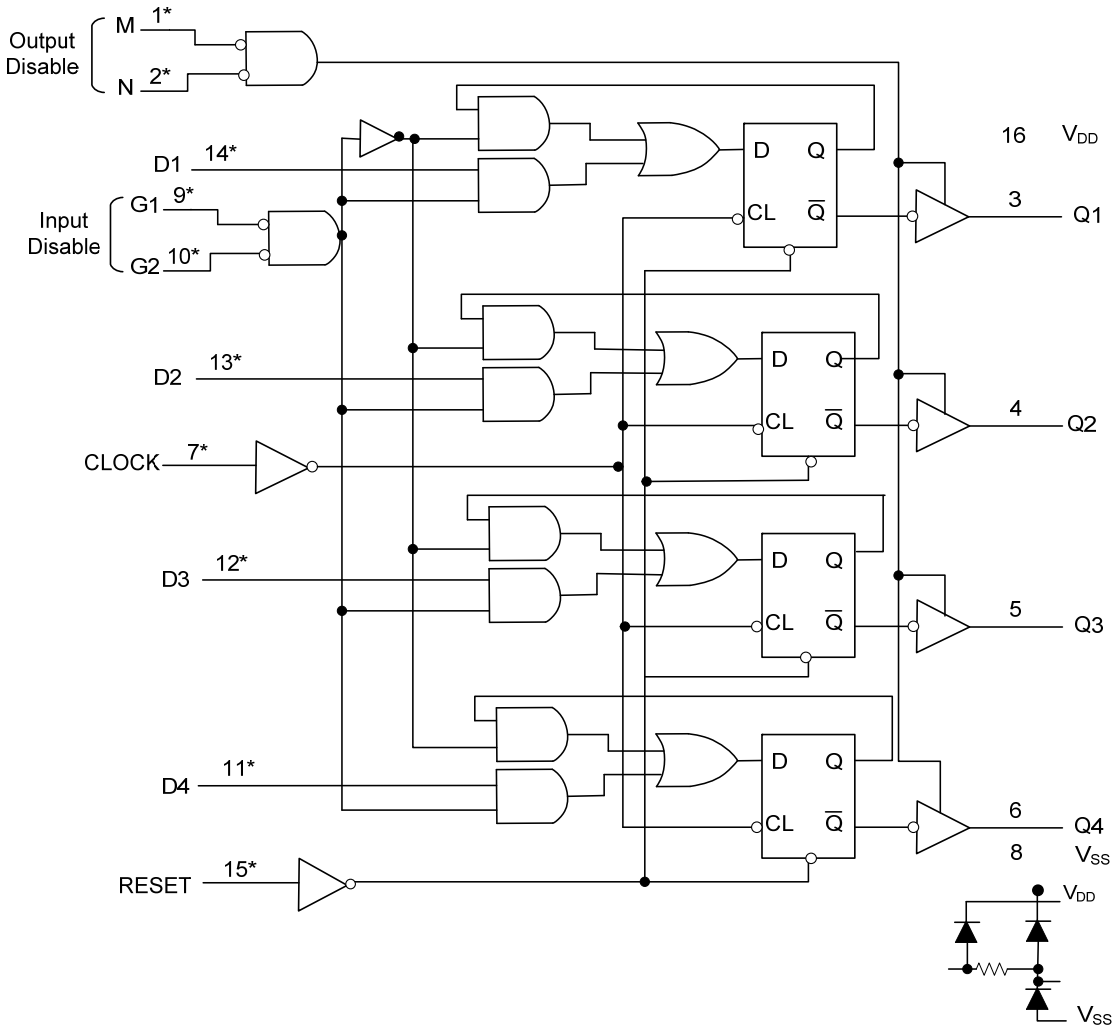


■ FUNCTION TABLE (each gate)

RESET	CLOCK	INPUT DISABLE (G1)	INPUT DISABLE (G2)	OUTPUT DISABLE (M)	OUTPUT DISABLE (N)	DATA(D)	OUTPUT(Q)	
H	X	X	X	X	X	X	L	
L	L	X	X	L	L	X	Q	NC
L	↑	H	X	L	L	X	Q	NC
L	↑	X	H	L	L	X	Q	NC
L	↑	L	L	L	L	H	H	
L	↑	L	L	L	L	L	L	
L	H	X	X	L	L	X	Q	NC
L	↓	X	X	L	L	X	Q	NC
L	X	X	X	H	X	X	Z	
L	X	X	X	X	H	X	Z	

Note: H: HIGH Voltage Level, L: LOW Voltage Level, X: Valid H or L, NC: No Change

■ LOGIC DIAGRAM (positive logic)



Note: " * " All input protected by CMOS protection network

■ ABSOLUTE MAXIMUM RATING (V_{SS}=0V, unless otherwise specified.)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.5 ~ +20	V
Input Voltage	V_{IN}	-0.5 ~ V_{DD}+0.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{DD}		3		18	V
Operating Temperature	T_{OPR}		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	V_{DD}=5V, V_O=0.5V	3.5			V
		V_{DD}=10V, V_O=1.0V	7.0			
		V_{DD}=15V, V_O=1.5V	11.0			
Low-Level Input Voltage	V_{IL}	V_{DD}=5V, V_O=4.5V			1.5	V
		V_{DD}=10V, V_O=9.0V			3.0	
		V_{DD}=15V, V_O=13.5V			4.0	
High-Level Output Voltage	V_{OH}	V_{DD}= 5V, No Load	4.95	5		V
		V_{DD}= 10V, No Load	9.95	10		
		V_{DD}= 15V, No Load	14.95	15		
Low-Level Output Voltage	V_{OL}	V_{DD}= 5V, No Load		0	0.05	V
		V_{DD}= 10V, No Load		0	0.05	
		V_{DD}= 15V, No Load		0	0.05	
High-Level Output Current (NOTE)	I_{OH}	V_{DD}=5V, V_O=4.6V	-0.51	-1		mA
		V_{DD}=5V, V_O=2.5V	-1.6	-3.2		
		V_{DD}=10V, V_O=9.5V	-1.3	-2.6		
		V_{DD}=15V, V_O=13.5V	-3.4	-6.8		
Low-Level Output Current (NOTE)	I_{OL}	V_{DD}=5V, V_O=0.4V	0.51	1		
		V_{DD}=10V, V_O=0.5V	1.3	2.6		
		V_{DD}=15V, V_O=1.5V	3.4	6.8		
Input Leakage Current	$I_{I(LEAK)}$	V_{DD}=18V, V_{IN}=V_{DD} or GND			±0.1	μA
Quiescent Supply Current	I_{DD}	V_{DD}=5V, V_{IN}=V_{DD} or V_{SS}, I_{OUT}=0		0.04	5	μA
		V_{DD}=10V, V_{IN}=V_{DD} or V_{SS}, I_{OUT}=0		0.04	10	
		V_{DD}=15V, V_{IN}=V_{DD} or V_{SS}, I_{OUT}=0		0.04	20	
		V_{DD}=20V, V_{IN}=V_{DD} or V_{SS}, I_{OUT}=0		0.08	100	

Note: I_{OL} and I_{OH} are tested one output at a time.

■ SWITCHING CHARACTERISTICS

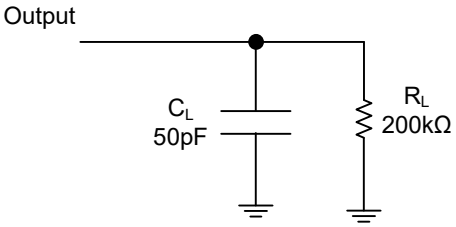
(Input: t_R=t_F=20ns, C_L=50pF, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation delay from Input(G1 or G2) to Output(Q)	t_{PLH}	V_{DD}=5V	R_L=200KΩ		300	600	ns
		V_{DD}=10V			125	250	
		V_{DD}=15V			90	180	
	t_{PHL}	V_{DD}=5V			230	460	
		V_{DD}=10V			100	200	
		V_{DD}=15V			75	150	
Transition Time	t_{TLH} t_{THL}	V_{DD}=5V			100	200	ns
		V_{DD}=10V			50	100	
		V_{DD}=15V			40	80	
3-State Output 1 Or 0 To High Impedance	t_{PHZ} t_{PLZ}	V_{DD}=5V	R_L=1KΩ		150	300	ns
		V_{DD}=10V			75	150	
		V_{DD}=15V			60	120	
3-State High Impedance To 1 Or 0 Output	t_{PZH} t_{PZL}	V_{DD}=5V			150	300	ns
		V_{DD}=10V			75	150	
		V_{DD}=15V			60	120	
Maximum Clock Input Frequency	f_{CL}	V_{DD}=5V	R_L=200KΩ	3	6		MHz
		V_{DD}=10V		6	12		
		V_{DD}=15V		8	16		
Maximum Clock Pluse Width	t_W	V_{DD}=5V			100	200	ns
		V_{DD}=10V			50	100	
		V_{DD}=15V			40	80	
Maximum Clock Input Rise Or Fall Time	t_{rcl} t_{fcl}	V_{DD}=5V		15			μs
		V_{DD}=10V		5			
		V_{DD}=15V		5			
Maximum Reset Pulse With	t_W	V_{DD}=5V			60	120	ns
		V_{DD}=10V			25	50	
		V_{DD}=15V			20	40	
Minimum Data Setup Time	t_S	V_{DD}=5V			100	200	ns
		V_{DD}=10V			40	80	
		V_{DD}=15V			30	60	
Minimum Data Input Disable Setup Time	t_S	V_{DD}=5V			90	180	ns
		V_{DD}=10V			50	100	
		V_{DD}=15V			35	70	

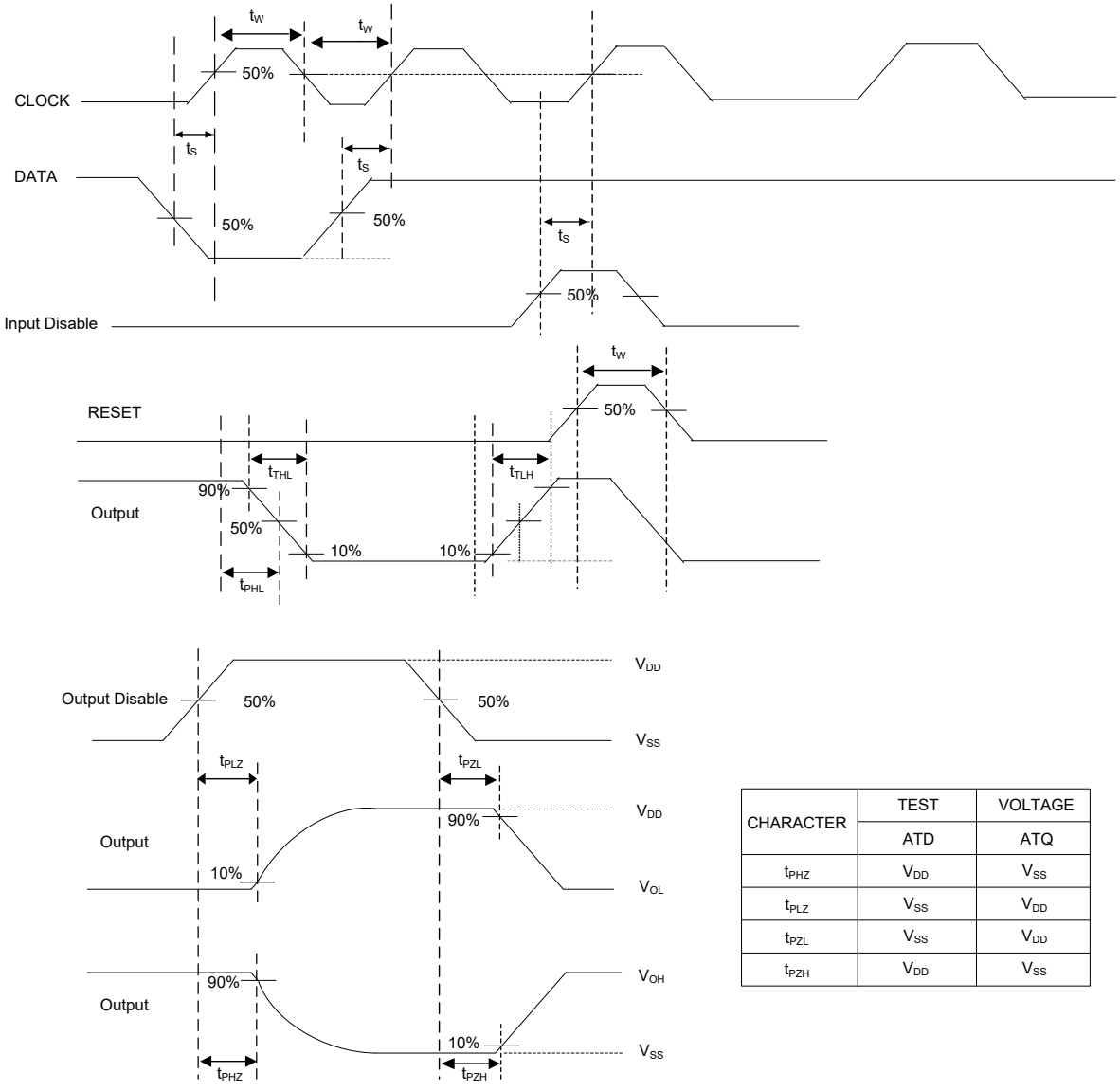
■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average Input Capacitance	C_{IN}	Any Input		5	7.5	pF

■ TEST CIRCUIT AND WAVEFORMS



TEST CIRCUIT



CHARACTER	TEST	VOLTAGE
	ATD	ATQ
t_{PHZ}	V_{DD}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}

VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

Note: C_L includes probe and jig capacitance.