



7N120-E4

Preliminary

Power MOSFET

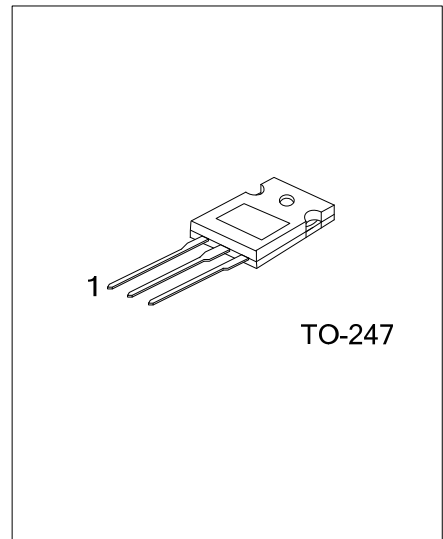
**7.0A, 1200V N-CHANNEL
POWER MOSFET**

■ DESCRIPTION

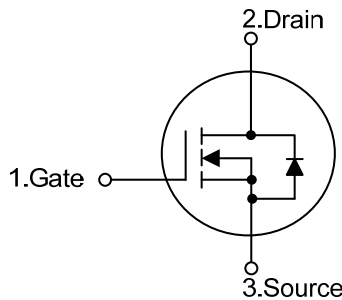
The UTC **7N120-E4** provide excellent $R_{DS(ON)}$, low gate charge and operation with low gate voltages. This device is suitable for use as a load switch or in PWM applications.

■ FEATURES

- * $R_{DS(ON)} \leq 2.6 \Omega @ V_{GS}=10V, I_D=3.5A$
- * Low Reverse Transfer Capacitance
- * Fast Switching Capability
- * Avalanche Energy Specified
- * Improved dv/dt Capability, High Ruggedness



■ SYMBOL



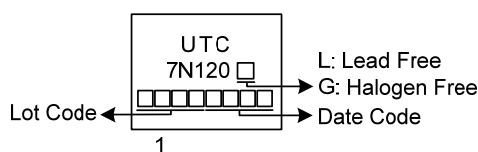
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
7N120L-T47-T	7N120G-T47-T	TO-247	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>7N120G-T47-T</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) T: Tube (2) T47: TO-247 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	1200	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	Continuous	I_D	7	A
	Pulsed (Note 2)	I_{DM}	14	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	352	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	1.65	V/ns
Power Dissipation		P_D	171	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L=30\text{mH}$, $I_{AS}=4.85\text{A}$, $V_{DD}=120\text{V}$, $R_G=25\ \Omega$, Starting $T_J = 25^\circ\text{C}$

4. $I_{SD} \leq 7.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	50	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	0.73	$^\circ\text{C}/\text{W}$

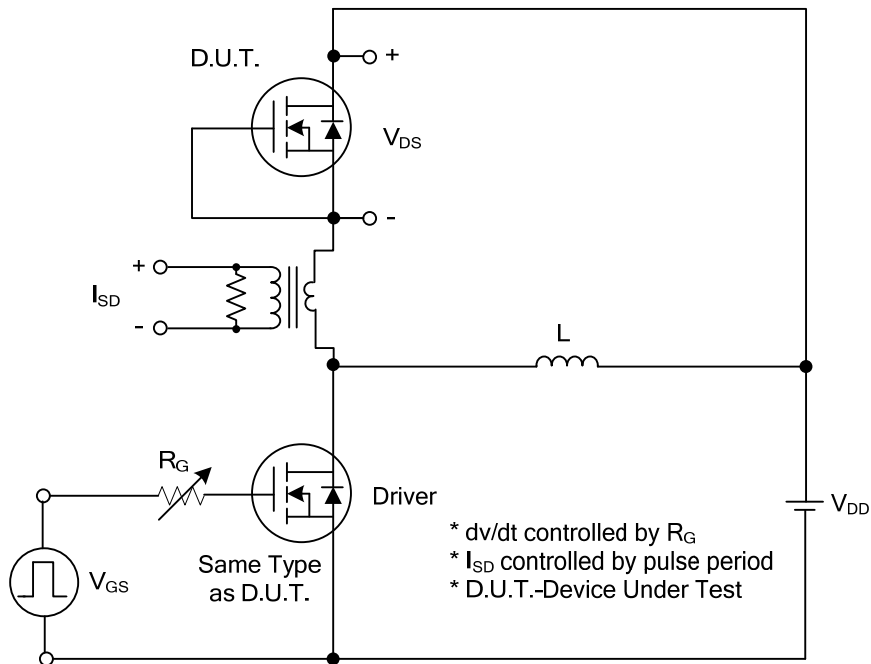
■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	1200			V	
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=1200\text{V}$, $V_{GS}=0\text{V}$			10	μA	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 30\text{V}$, $V_{DS}=0\text{V}$			± 100	nA	
ON CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	3.0		5.0	V	
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=3.5\text{A}$			2.6	Ω	
DYNAMIC CHARACTERISTICS							
Input Capacitance	C_{ISS}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$		1490		pF	
Output Capacitance	C_{OSS}				164		pF
Reverse Transfer Capacitance	C_{RSS}				55		pF
SWITCHING CHARACTERISTICS							
Total Gate Charge (Note 1)	Q_G	$V_{DS}=960\text{V}$, $V_{GS}=10\text{V}$, $I_D=7.0\text{A}$ (Note 1, 2)		77		nC	
Gate-Source Charge	Q_{GS}			21		nC	
Gate-Drain Charge	Q_{GD}			35		nC	
Turn-On Delay Time (Note 1)	$t_{D(ON)}$	$V_{DD}=100\text{V}$, $V_{GS}=10\text{V}$, $I_D=7.0\text{A}$, $R_G=25\ \Omega$ (Note 1, 2)		28		ns	
Turn-On Rise Time	t_R			34		ns	
Turn-Off Delay Time	$t_{D(OFF)}$			208		ns	
Turn-Off Fall Time	t_F			70		ns	
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS							
Maximum Continuous Drain-Source Diode Forward Current	I_S				7	A	
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				14	A	
Drain-Source Diode Forward Voltage (Note 1)	V_{SD}	$I_S=7.0\text{A}$, $V_{GS}=0\text{V}$			1.4	V	
Body Diode Reverse Recovery Time (Note 1)	t_{rr}	$I_S=7.0\text{A}$, $V_{GS}=0\text{V}$,		960		nS	
Body Diode Reverse Recovery Charge	Q_{rr}	$dI_F/dt=100\text{A}/\mu\text{s}$		14.6		μC	

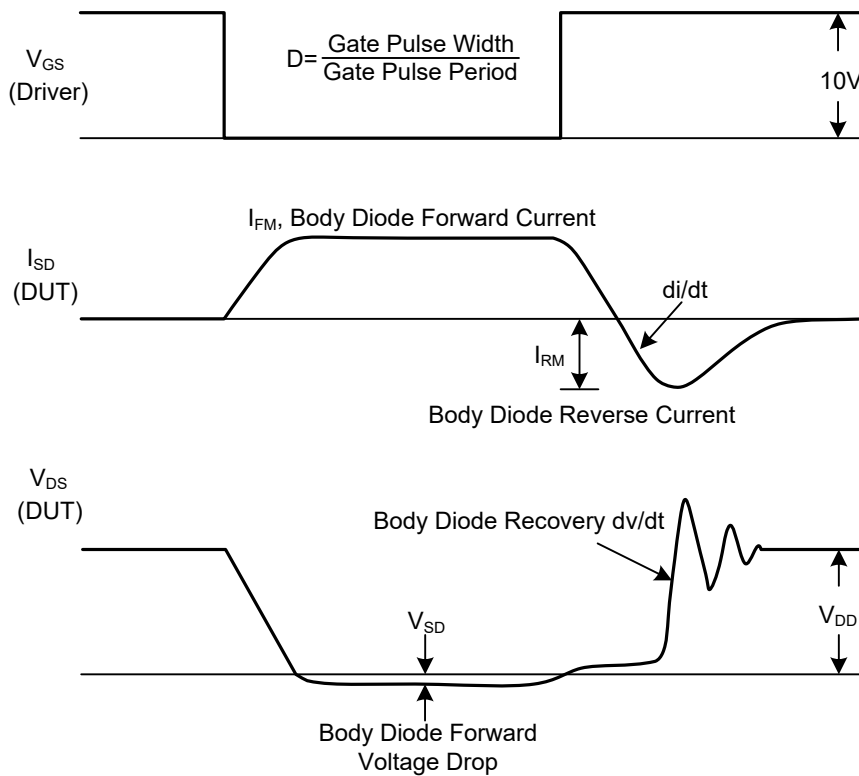
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

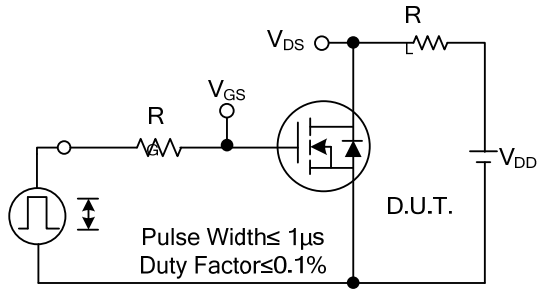


Peak Diode Recovery dv/dt Test Circuit

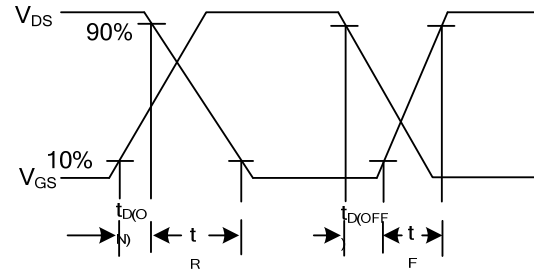


Peak Diode Recovery dv/dt Waveforms

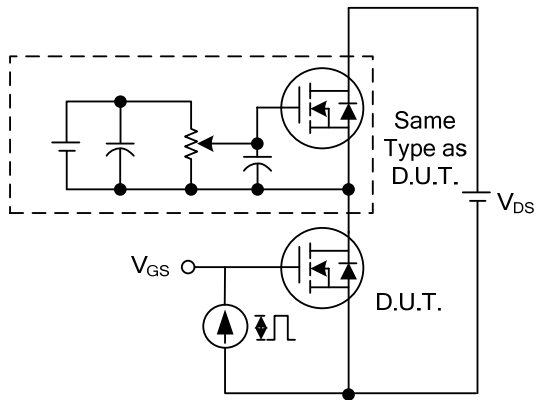
■ TEST CIRCUITS AND WAVEFORMS



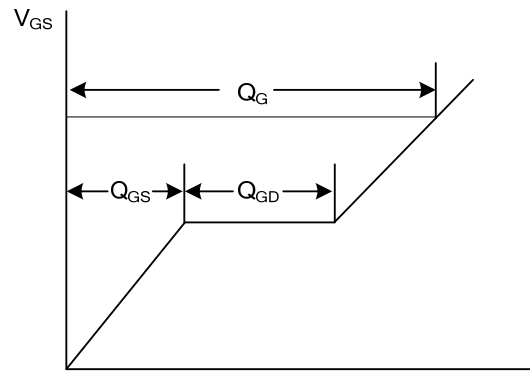
Switching Test Circuit



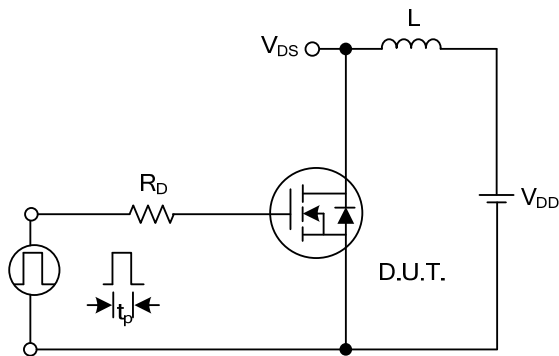
Switching Waveforms



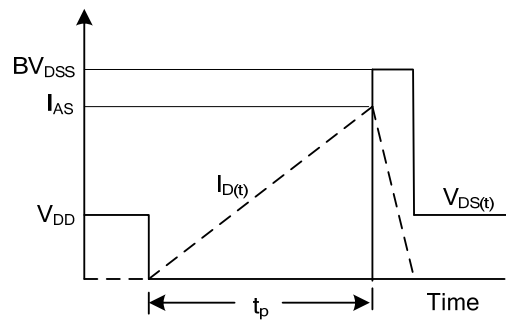
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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