



2NM120

Preliminary

Power MOSFET

2.0A, 1200V N-CHANNEL SUPER-JUNCTION MOSFET

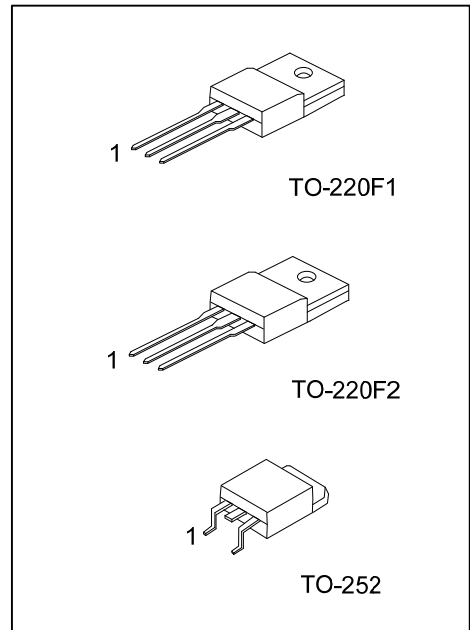
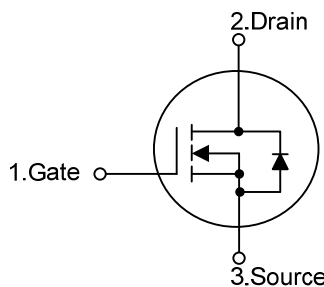
■ DESCRIPTION

The UTC **2NM120** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at AC-DC converters for power applications.

■ FEATURES

- * $R_{DS(ON)} \leq 6.2 \Omega @ V_{GS}=10V, I_D=1.0A$
- * High Switching Speed

■ SYMBOL



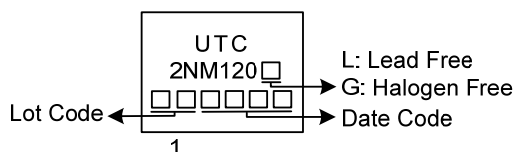
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2NM120L-TF1-T	2NM120G-TF1-T	TO-220F1	G	D	S	Tube
2NM120L-TF2-T	2NM120G-TF2-T	TO-220F2	G	D	S	Tube
2NM120L-TN3-R	2NM120G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>2NM120G-TF1-T</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) TF1: TO-220F1, TF2: TO-220F2, TN3: TO-252</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
----------------------	--

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	1200	V
Gate-Source Voltage	V_{GSS}	± 30	V
Continuous Drain Current	Continuous	I_D	2
	Pulsed	I_{DM}	4
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	60
Peak Diode Recovery dv/dt (Note 4)	dv/dt	2.5	V/ns
Power Dissipation	TO-220F1	P_D	21
	TO-220F2		
	TO-252		23
Junction Temperature	T_J	+150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^{\circ}\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 100\text{mH}$, $I_{AS} = 1.09\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\ \Omega$ Starting $T_J = 25^{\circ}\text{C}$

4. $I_{SD} \leq 2.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^{\circ}\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	62.5	$^{\circ}\text{C}/\text{W}$
		110	$^{\circ}\text{C}/\text{W}$
Junction to Case	θ_{JC}	5.95	$^{\circ}\text{C}/\text{W}$
		5.43(Note)	$^{\circ}\text{C}/\text{W}$

Note: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

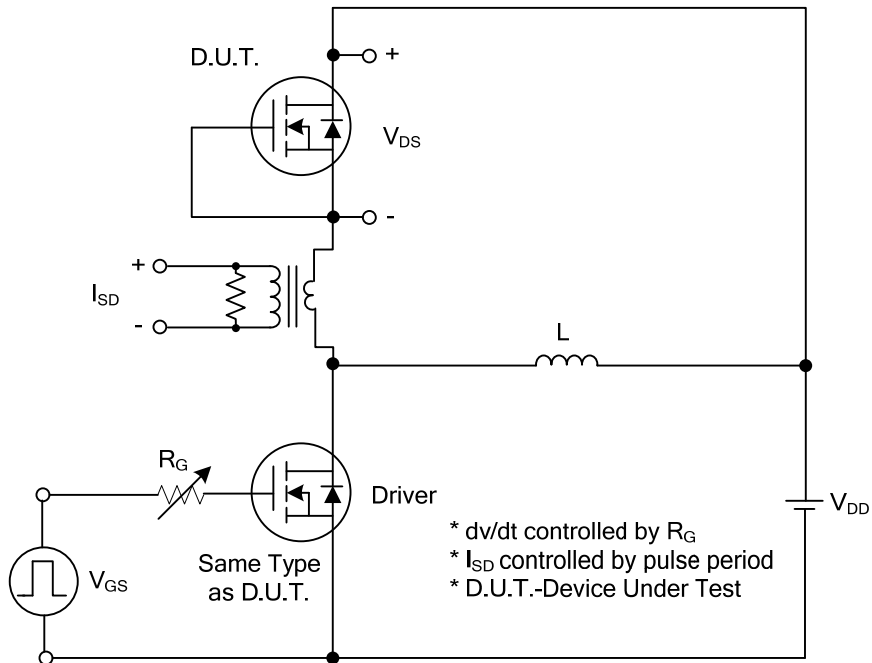
■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D=250\mu A, V_{GS}=0V$	1200			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=1200V, V_{GS}=0V$			10	μA
Gate-Source Leakage Current	Forward	I_{GSS}			+100	nA
	Reverse				-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5		4.5	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=1.0A$			6.2	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0V, V_{DS}=50V, f=1.0MHz$		245		pF
Output Capacitance	C_{OSS}			20		pF
Reverse Transfer Capacitance	C_{RSS}			2.3		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{DS}=960V, V_{GS}=10V, I_D=2.0A$ (Note 1, 2)		16		nC
Gate to Source Charge	Q_{GS}			6		nC
Gate to Drain Charge	Q_{GD}			3		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=100V, V_{GS}=10V, I_D=2.0A,$ $R_G=25\Omega$ (Note 1, 2)		5.6		ns
Rise Time	t_R			17		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			36		ns
Fall-Time	t_F			40		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				2	A
Maximum Body-Diode Pulsed Current	I_{SM}				4	A
Drain-Source Diode Forward Voltage	V_{SD}	$I_S=2.0A, V_{GS}=0V$			1.4	V
Body Diode Reverse Recovery Time	t_{rr}	$I_S=2.0A, V_{GS}=0V,$ $dI_F/dt=100A/\mu s$ (Note 1)		470		ns
Reverse Recovery Charge	Q_{rr}			2.9		μC

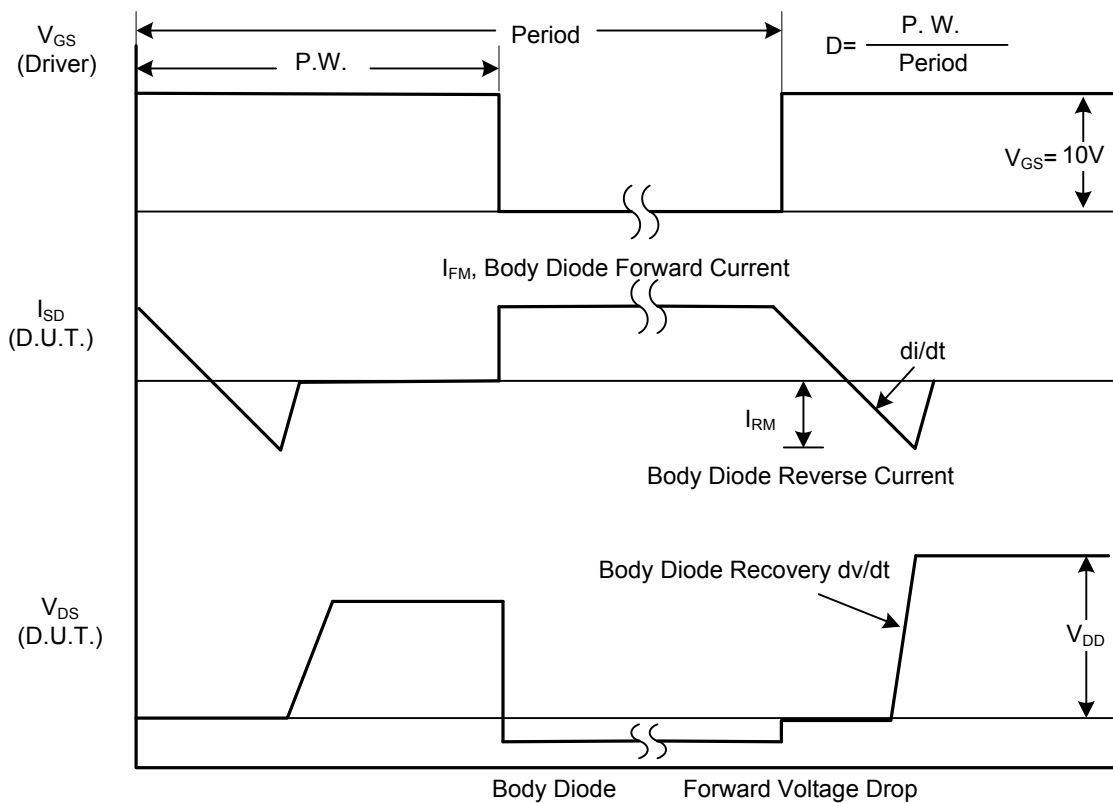
Notes: 1. Pulse Test: Pulse width $\leq 1200\mu s$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

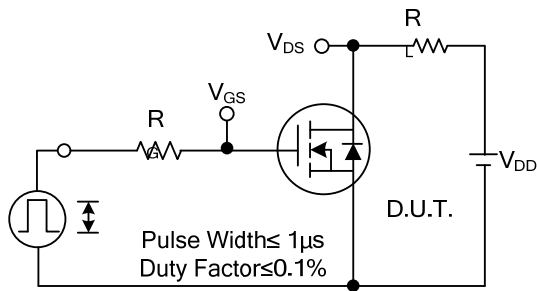


Peak Diode Recovery dv/dt Test Circuit

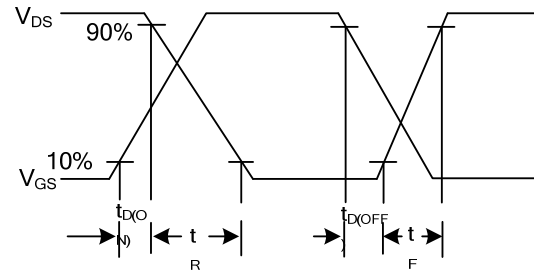


Peak Diode Recovery dv/dt Waveforms

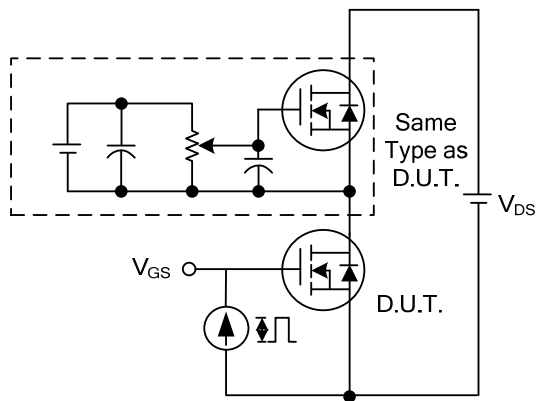
■ TEST CIRCUITS AND WAVEFORMS



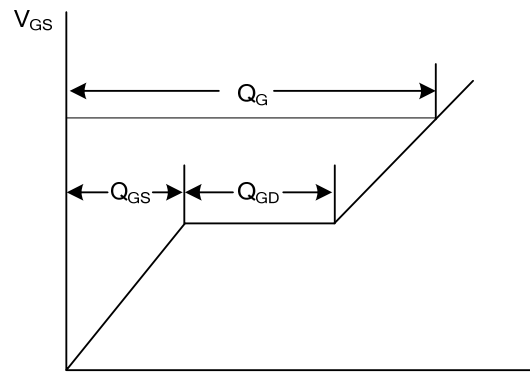
Switching Test Circuit



Switching Waveforms

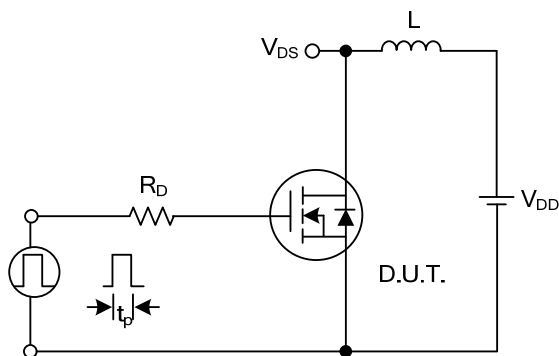


Gate Charge Test Circuit

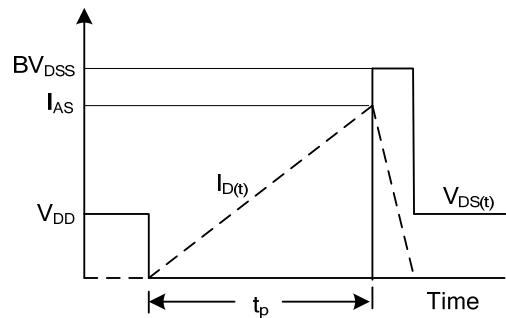


Charge

Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.