



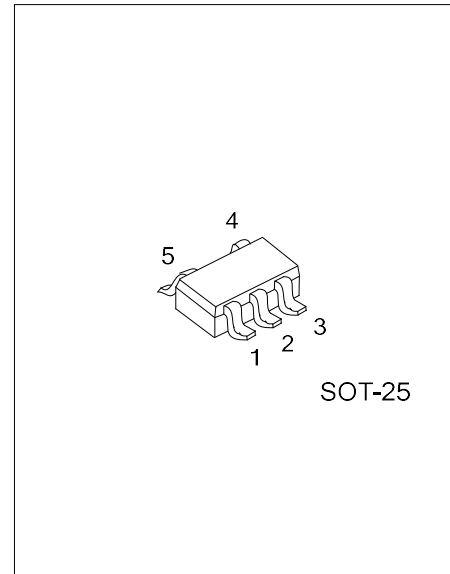
SPST CMOS ANALOG SWITCHES

DESCRIPTION

The UTC **US12A4515** are single pole/single throw (SPST), low-voltage, single-supply CMOS analog switches, with very low switch ON-state resistance. The **US12A4515** is normally closed (NC).

These CMOS switches can operate continuously with a single supply between 2V and 12V. Each switch can handle rail-to-rail analog signals.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a 5V supply.



FEATURES

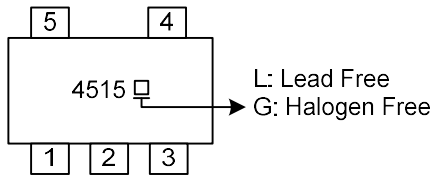
- * 2V to 12V Single-Supply Operation
- * Specified ON-State Resistance:
 - 15Ω Max With 12V Supply
 - 20Ω Max With 5V Supply
 - 50Ω Max With 3.3V Supply
- * Low Charge Injection: 11.5pC (12V Supply)
- * Fast Switching Speed:
 - t_{ON} = 80ns, t_{OFF} = 50ns (12V Supply)
- * Break-Before-Make Operation (t_{ON} > t_{OFF})
- * TTL/CMOS-Logic Compatible With 5V Supply

ORDERING INFORMATION

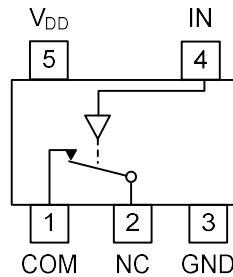
Ordering Number		Package	Packing
Lead Free	Halogen Free		
US12A4515L-AF5-R	US12A4515G-AF5-R	SOT-25	Tape Reel

US12A4515G-AF5-R	(1)Packing Type	(1) R: Tape Reel
	(2)Package Type	(2) AF5: SOT-25
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

MARKING



PIN CONFIGURATION



PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	COM	Common
2	NC	Normally closed
3	GND	Digital ground
4	IN	Digital control to connect COM to NO or NC
5	V _{DD}	Power supply

Note: NO, NC, and COM pins are identical and interchangeable. Any may be considered as an input or an output; signals pass in both directions.

FUNCTION TABLE

INPUT	SWITCH STATE
LOW	ON
HIGH	OFF

■ ABSOLUTE MAXIMUM RATING (Note 1, 2)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (Note 3)	V_{DD}	-0.3 ~ 13	V
Analog Voltage range (Note 4)	V_{NC} V_{COM}	-0.3 ~ $V_{DD}+0.3$ or $\pm 20\text{mA}$	V
Continuous Current into any Terminal $\pm 20\text{mA}$		± 20	mA
Peak current, COM (Pulsed at 1 ms, 10% duty cycle)		± 30	mA
Continuous Power Dissipation ($T_A=70^\circ\text{C}$)	P_D	360	mW
Operating Temperature Range	T_{OPR}	-40 ~ +85	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-65 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
3. All voltages are with respect to ground, unless otherwise specified.
4. Voltages exceeding $V+$ or GND on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

■ ELECTRICAL CHARACTERISTICS FOR 3V SUPPLY (Note 1)

($V_{DD}=3.0V$ to $3.6V$, $V_{INH}=2.4V$, $V_{INL}=0.8V$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25^\circ C$			$-40^\circ C \sim +85^\circ C$			UNIT
			MIN	TYP (Note 2)	MAX	MIN	TYP	MAX	
ANALOG SWITCH									
Analog Signal Range	V_{COM} V_{NC}	$V_{DD}=3V$, $V_{COM}=1.5V$, $I_{NO}=1mA$	0		V_{DD}	0		V_{DD}	V
ON-state Resistance	R_{ON}	$V_{DD}=3V$, $V_{COM}=1V$, $1.5V$, $2V$, $I_{COM}=1mA$		18.5	40			50	Ω
ON-state Resistance Flatness	$R_{ON(Flat)}$	$V_{DD}=3.6V$, $V_{COM}=1V$, $V_{NC}=3V$		1	3			4	Ω
NC OFF Leakage Current (Note 2)	$I_{NC(OFF)}$	$V_{DD}=3.6V$, $V_{COM}=1V$, $V_{NC}=3V$			100			200	nA
COM OFF Leakage Current (Note 2)	$I_{COM(OFF)}$	$V_{DD}=3.6V$, $V_{COM}=3V$, $V_{NC}=3V$			100			200	nA
COM ON Leakage Current (Note 2)	$I_{COM(ON)}$				100			200	nA
DIGITAL CONTROL INPUT (IN)									
Input Logic High	V_{IH}		2.4		V_{DD}	2.4		V_{DD}	V
Input Logic Low	V_{IL}		0		0.8	0		0.8	V
Input Leakage Current	I_{IH} , I_{IL}	$V_{IN} = V_{DD}$, $0V$			0.1			0.15	μA
DYNAMIC									
Turn-ON Time	t_{ON}	See Figure2		63	120			175	ns
Turn-OFF Time	t_{OFF}	See Figure2		33	80			120	ns
Charge Injection (Note 3)	Q_C	$C_L=1nF$, See Figure 1		-1.5					pC
NC OFF Capacitance	$C_{NC(OFF)}$	$f=1MHz$, See Figure 4		7.5					pF
COM OFF Capacitance	$C_{COM(OFF)}$	$f=1MHz$, See Figure 4		7.5					pF
COM ON Capacitance	$C_{COM(ON)}$	$f=1MHz$, See Figure 4		17					pF
Digital input Capacitance	C_i	$V_{IN} = V_{DD}$, $0V$		1.5					pF
Bandwidth	BW	$R_L=50\Omega$, $C_L=15pF$, $V_{NC}=1 V_{RMS}$, $f=100kHz$		460					MHz
OFF Isolation	O_{ISO}	$R_L=50\Omega$, $C_L=15pF$, $V_{NC}=1 V_{RMS}$, $f=100kHz$		-94					dB
Total Harmonic Distortion	THD	$R_L=50\Omega$, $C_L=15pF$, $V_{NC}=1 V_{RMS}$, $f=100kHz$		0.15					%
SUPPLY									
V_{DD} Supply Current	I_+	$V_{IN}=0V$ or V_{DD}			0.1			0.15	μA

Notes: 1. The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

2. Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.

3. Specified by design, not production tested.

■ ELECTRICAL CHARACTERISTICS FOR 5V SUPPLY (Note 1)

($V_{DD}=4.5V$ to $5.5V$, $V_{INH}=2.4V$, $V_{INL}=0.8V$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25^\circ C$			$-40^\circ C \sim +85^\circ C$			UNIT
			MIN	TYP (Note 2)	MAX	MIN	TYP	MAX	
ANALOG SWITCH									
Analog Signal Range	V_{COM} V_{NC}	$V_{DD}=4.5V$, $V_{COM}=3.5V$, $I_{COM}=1mA$	0		V_{DD}	0		V_{DD}	V
ON-state Resistance	R_{ON}	$V_{COM}=1V, 2V, 3V$, $I_{COM}=1mA$		9.5	15			20	Ω
ON-state Resistance Flatness	$R_{ON(Flat)}$	$V_{DD}=5.5V$, $V_{COM}=1V$, $V_{NC}=4.5V$		1	3			4	Ω
NC OFF Leakage Current (Note 2)	$I_{NC(OFF)}$	$V_{DD}=5.5V$, $V_{COM}=1V$, $V_{NC}=4.5V$			100			200	nA
COM OFF Leakage Current (Note 2)	$I_{COM(OFF)}$	$V_{DD}=5.5V$, $V_{COM}=4.5V$, $V_{NC}=4.5V$			100			200	nA
COM ON Leakage Current (Note 2)	$I_{COM(ON)}$				100			200	nA
DIGITAL CONTROL INPUT (IN)									
Input Logic High	V_{IH}		2.4		V_{DD}	2.4		V_{DD}	V
Input Logic Low	V_{IL}		0		0.8	0		0.8	V
Input Leakage Current	I_{IH}, I_{IL}	$V_{IN} = V_{DD}, 0V$			0.1			0.15	μA
DYNAMIC									
Turn-ON Time	t_{ON}	See Figure2		32	100			125	ns
Turn-OFF Time	t_{OFF}	See Figure2		25	50			60	ns
Charge Injection (Note 3)	Q_C	$C_L=1nF$, $V_{NC}=0V$, $R_S=0\Omega$, See Figure1		-3					pC
NC OFF Capacitance	$C_{NC(OFF)}$	$f=1MHz$, See Figure 4		7.5					pF
COM OFF Capacitance	$C_{COM(OFF)}$	$f=1MHz$, See Figure 4		7.5					pF
COM ON Capacitance	$C_{COM(ON)}$	$f=1MHz$, See Figure 4		19					pF
Digital input Capacitance	C_i	$V_{IN} = V_{DD}, 0V$		1.5					pF
Bandwidth	BW	$R_L=50\Omega$, $C_L=15pF$, $V_{NC}=1V_{RMS}$, $f=100kHz$		475					MHz
OFF Isolation	O_{ISO}	$R_L=50\Omega$, $C_L=15pF$, $V_{NC}=1V_{RMS}$, $f=100kHz$		-94					dB
Total Harmonic Distortion	THD	$R_L=50\Omega$, $C_L=15pF$, $V_{NC}=1V_{RMS}$, $f=100kHz$		0.08					%
SUPPLY									
V_{DD} Supply Current	I_+	$V_{IN}=0V$ or V_{DD}			0.15			0.2	μA

Notes: 1. The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

2. Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.

3. Specified by design, not production tested.

■ ELECTRICAL CHARACTERISTICS FOR 12V SUPPLY (Note 1)

($V_{DD}=11.4V$ to $12.6V$, $V_{INH}=5V$, $V_{INL}=0.8V$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A=25^{\circ}C$			$-40^{\circ}C\sim+85^{\circ}C$			UNIT
			MIN	TYP (Note 2)	MAX	MIN	TYP	MAX	
ANALOG SWITCH									
Analog Signal Range	V_{COM} V_{NC}	$V_{DD}=11.4V$, $V_{COM}=10V$, $I_{COM}=1mA$	0		V_{DD}	0		V_{DD}	V
ON-state Resistance	R_{ON}	$V_{COM}=11.4V$, 2V, 5V, 10V, $I_{COM}=1mA$		6.5	10			15	Ω
ON-state Resistance Flatness	$R_{ON(Flat)}$	$V_{DD}=12.6V$, $V_{COM}=1V$, $V_{NC}=10V$		1.5	3			4	Ω
NC OFF Leakage Current (Note 2)	$I_{NC(OFF)}$	$V_{DD}=12.6V$, $V_{COM}=1V$, $V_{NC}=10V$			100			200	nA
COM OFF Leakage Current (Note 2)	$I_{COM(OFF)}$	$V_{DD}=12.6V$, $V_{COM}=10V$, $V_{NC}=10V$			100			200	nA
COM ON Leakage Current (Note 2)	$I_{COM(ON)}$				100			200	nA
DIGITAL CONTROL INPUT (IN)									
Input Logic High	V_{IH}		5		V_{DD}	5		V_{DD}	V
Input Logic Low	V_{IL}		0		0.8	0		0.8	V
Input Leakage Current	I_{IH} , I_{IL}	$V_{IN} = V_{DD}$, 0V			0.1			0.15	μA
DYNAMIC									
Turn-ON Time	t_{ON}	See Figure2		22	75			80	ns
Turn-OFF Time	t_{OFF}	See Figure2		20	45			50	ns
Charge Injection (Note 3)	Q_C	$C_L=1nF$, $V_{NC}=0V$, $R_S=0\Omega$ See Figure1		-11.5					pC
NC OFF Capacitance	$C_{NC(OFF)}$	$f=1MHz$, See Figure 4		7.5					pF
COM OFF Capacitance	$C_{COM(OFF)}$	$f=1MHz$, See Figure 4		7.5					pF
COM ON Capacitance	$C_{COM(ON)}$	$f=1MHz$, See Figure 4		21.5					pF
Digital input Capacitance	C_i	$V_{IN} = V_{DD}$, 0V		1.5					pF
Bandwidth	BW	$R_L=50\Omega$, $C_L=15pF$, $V_{NC}=1 V_{RMS}$, $f=100kHz$		520					MHz
OFF Isolation	O_{ISO}	$R_L=50\Omega$, $C_L=15pF$, $V_{NC}=1 V_{RMS}$, $f=100kHz$		-95					dB
Total Harmonic Distortion	THD	$R_L=50\Omega$, $C_L=15pF$, $V_{NC}=1 V_{RMS}$, $f=100kHz$		0.07					%
SUPPLY									
V_{DD} Supply current	I_+	$V_{IN}=0V$ or V_{DD}			0.15			0.2	μA

Notes: 1. The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

2. Leakage parameters are 100% tested at maximum-rated hot operating temperature, and are ensured by correlation at 25°C.

3. Specified by design, not production tested.

■ TEST CIRCUITS / TIMING DIAGRAMS

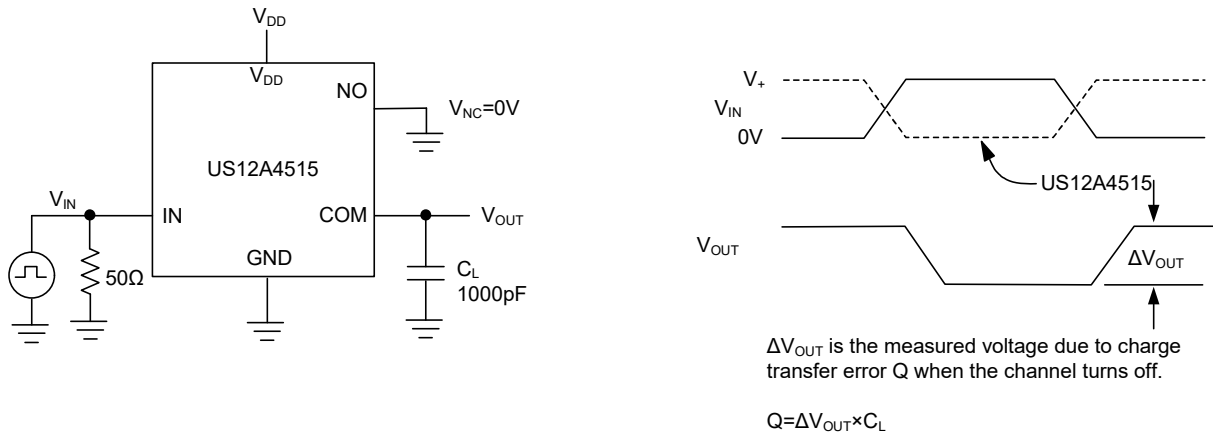


Figure 1. Charge Injection

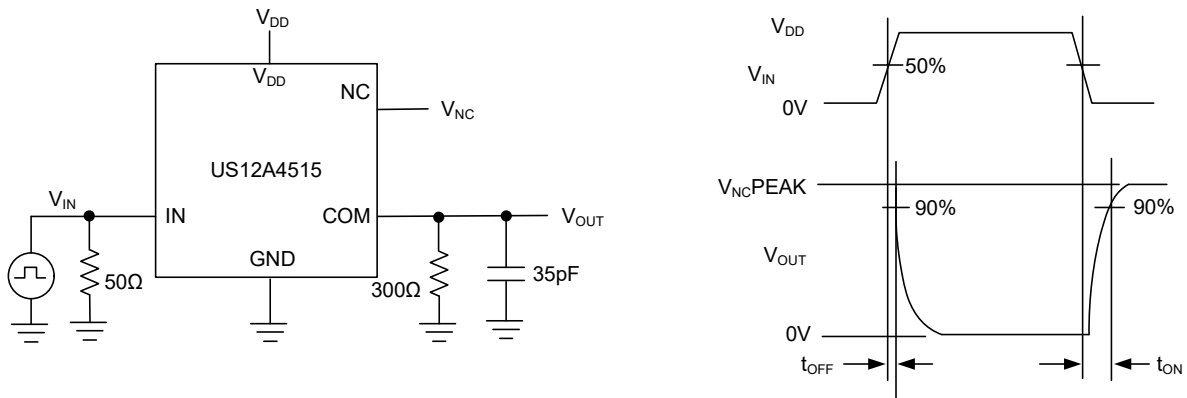
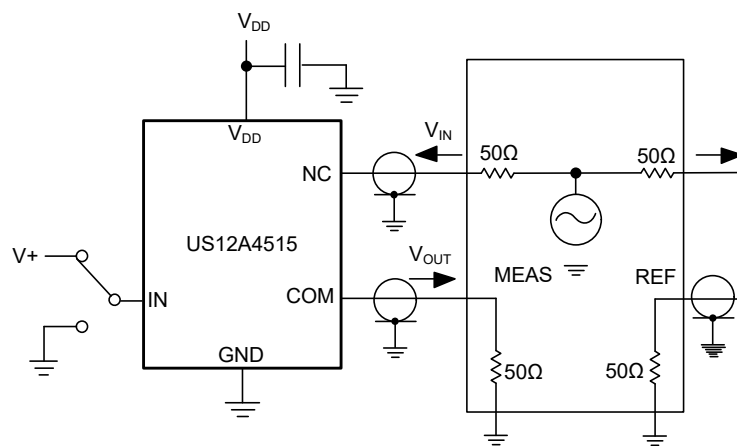


Figure 2. Switching Times



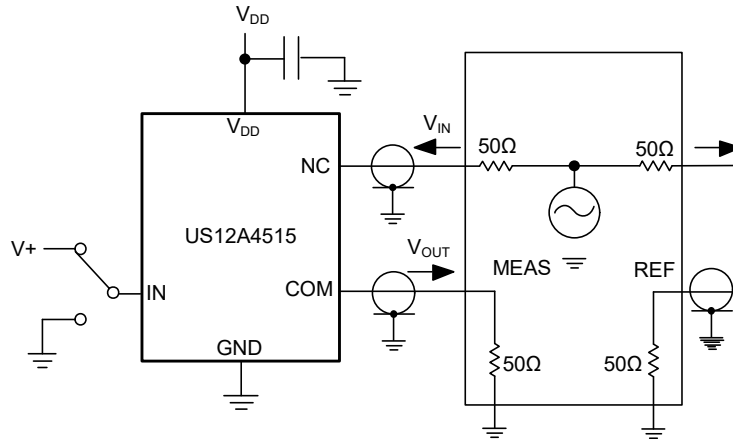
Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. ON loss is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

$$\text{OFF Isolation} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

$$\text{ON Loss} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

Figure 3. OFF Isolation and ON Loss

■ TEST CIRCUITS / TIMING DIAGRAMS (Cont.)



Measurements are standardized against short at socket terminals. OFF isolation is measured between COM and OFF terminals on each switch. ON loss is measured between COM and ON terminals on each switch. Signal direction through switch is reversed; worst values are recorded.

$$\text{OFF Isolation} = 20 \log \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

$$\text{ON Loss} = 20 \log \frac{V_{\text{OUT}}}{V_{\text{IN}}}$$

Figure 3. OFF Isolation and ON Loss

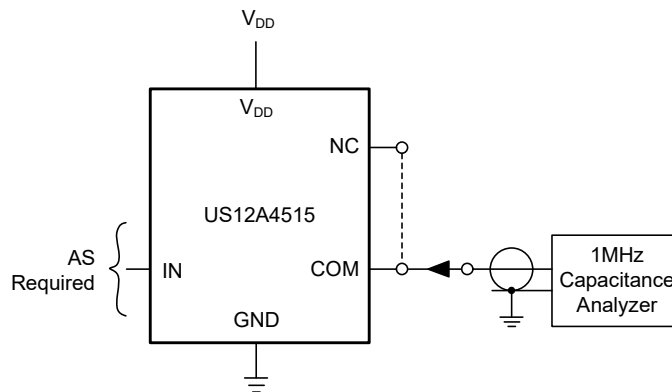


Figure 4. NO, NC, and COM Capacitance

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