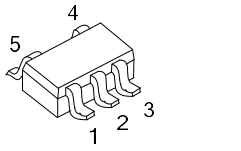
2N7001 **Preliminary** ***CMOS IC***

SINGLE-BIT DUAL-SUPPLY BUFFERED VOLTAGE SIGNAL CONVERTER



SOT-353

■ DESCRIPTION

The UTC **2N7001** is a single-bit buffered voltage signal converter that uses two separate configurable powersupply rails to up or down translate a unidirectional signal. The device is operational with both V_{CCA} and V_{CCB} supplies down to 1.65 V and up to 3.60 V. V_{CCA} defines the input threshold voltage on the A input. V_{CCB} defines the output drive voltage on the B output.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry ensures that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specific voltage while the device is powered down.

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} is less than 100 mV, the output port (B) enters a high-impedance state.

■ FEATURES

* Up and down translation across 1.65V to 3.6V
* Maximum quiescent current (I_{CCA} + I_{CCB}) of 14μA (125°C maximum)
* V_{CC} isolation feature
  If either V_{CC} input is below 100 mV, the output becomes high-impedance
* I_{OFF} supports partial-power-down mode operation

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
2N7001L-AL5-R	2N7001G-AL5-R	SOT-353	Tape Reel

2N7001G-AL5-R
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) AL5: SOT-353
(3) G: Halogen Free and Lead Free, L: Lead Free

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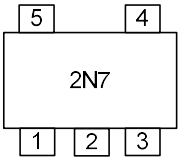
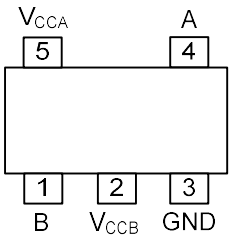
■ MARKING



■ PIN CONFIGURATION



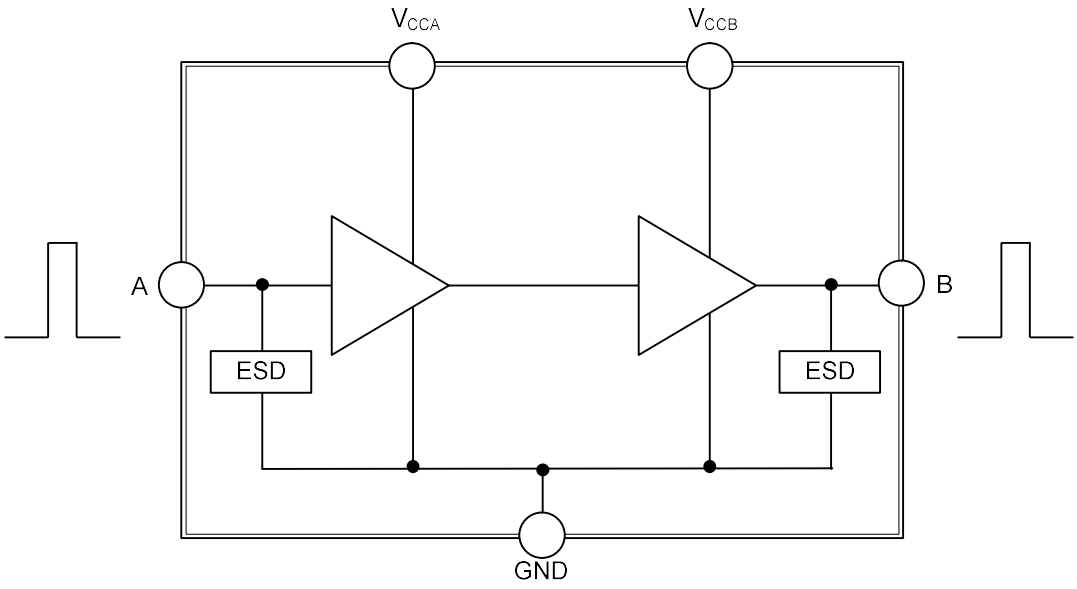
■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	B	Data Output. This pin is referenced to V_{CCB}
2	V_{CCB}	Output Supply voltage. 1.65V ≤ V_{CCB} ≤ 3.6V
3	GND	Ground
4	A	Data Input. This pin is referenced to V_{CCA}
5	V_{CCA}	Input Supply voltage. 1.65V ≤ V_{CCA} ≤ 3.6V

■ FUNCTION TABLE

INPUT	OUTPUT
L (Referenced to V_{CCA})	L (Referenced to V_{CCB})
H (Referenced to V_{CCA})	H (Referenced to V_{CCB})

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING [over operating free-air temperature range (unless otherwise noted)]

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage, A Port		V_{CCA}	-0.5 ~ 4.2	V
Supply Voltage, B Port		V_{CCB}	-0.5 ~ 4.2	V
Input Voltage (Note2)		V_I	-0.5 ~ 4.2	V
Voltage Applied to the Output in the High-Impedance or Power-Off State (Note 2)		V_O	-0.5 ~ 4.2	V
Voltage Applied to the Output in the High or Low State (Note 2, 3)		V_O	-0.5 ~ V_{CCB}+0.2	V
Input Clamp Current	V_I<0		-50	mA
Output Clamp Current	V_O<0		-50	mA
Continuous Output Current		I_O	-50 ~ 50	mA
Continuous Current Through V_{CCB} or GND		I_O	-50 ~ 50	mA
Continuous Current Through V_{CCA}		I_O	-10 ~ 10	mA
Operating Junction Temperature		T_J	-40 ~ +150	°C
Storage Temperature		T_{STG}	-65 ~ +160	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. The output positive-voltage rating may be exceeded up to 4.2 V maximum if the output current ratings are observed

■ RECOMMENDED OPERATING CONDITIONS

[over operating free-air temperature range (unless otherwise noted)]

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage, V_{CCA}	V_{CCA}		1.65		3.6	V
Supply Voltage, V_{CCB}	V_{CCB}		1.65		3.6	V
Input Voltage	V_I		0		3.6	V
Output Voltage	V_O	Active state	0		V_{CCB}	V
		Tri-sate	0		3.6	
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$				100	ns/V
Operating Free-Air Temperature	T_A		-40		+125	°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	350	°C/W

■ ELECTRICAL CHARACTERISTICS (T_A=-40~+125°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
High-Level Input Voltage	V_{IH}	V_{CCA} = 1.65 V - 1.95 V		V_{CCA} ×0.65			V
		V_{CCA} = 2.30 V – 2.70 V		1.60			V
		V_{CCA} = 3.00 V – 3.60 V		2.00			V
Low-Level Input Voltage	V_{IL}	V_{CCA} = 1.65 V - 1.95 V				V_{CCA} ×0.35	V
		V_{CCA} = 2.30 V – 2.70 V				0.70	V
		V_{CCA} = 3.00 V – 3.60 V				0.80	V
High-Level Output Voltage	V_{OH}	V_{CCA}=1.65V~3.6V, V_{CCB}=1.65V~3.6V, I_{OH}=–100μA		V_{CCB}-0.1			V
		V_{CCA}=1.65V, V_{CCB}=1.65V, I_{OH}=–8mA		1.2			V
		V_{CCA}=2.3V, V_{CCB}=2.3V,I_{OH}=–9mA		1.75			V
		V_{CCA}=3V, V_{CCB}=3V,I_{OH}=–12mA		2.3			V
Low-Level Output Voltage	V_{OL}	V_{CCA}=1.65V~3.6V, V_{CCB}=1.65V~3.6V, I_{OH}=100μA				0.1	V
		V_{CCA}=1.65V, V_{CCB}=1.65V, I_{OH}=8mA				0.45	V
		V_{CCA}=2.3V, V_{CCB}=2.3V,I_{OH}=9mA				0.55	V
		V_{CCA}=3V, V_{CCB}=3V,I_{OH}=12mA				0.7	V
Partial Power Down Current	I_{off}	V_{CCA}=0V, V_{CCB}=0V~3.6V, V_I or V_O=0V-3.6V		-8		8	μA
		V_{CCA}=0V~3.6V, V_{CCB}=0V, V_I or V_O=0V-3.6V		-8		8	μA
V_{CCA} Supply Current	I_{CCA}	V_I=V_{CCA} or GND I_O=0mA	V_{CCA}=1.65V~3.6V V_{CCB}=1.65V~3.6V			8	μA
			V_{CCA}=0V V_{CCB}=0V~3.6V	-8			μA
			V_{CCA}=0V~3.6V V_{CCB}=0V			8	μA
V_{CCB} Supply Current	I_{CCB}	V_I=V_{CCI} or GND I_O=0mA	V_{CCA}=1.65V~3.6V V_{CCB}=1.65V~3.6V			8	μA
			V_{CCA}=0V V_{CCB}=0V~3.6V			8	μA
			V_{CCA}=0V~3.6V V_{CCB}=0V	-8			μA
Combined Supply Current	I_{CCA} + I_{CCB}	V_{CCA}=1.65V~3.6V, V_{CCB}=1.65V~3.6V, V_I=V_{CCI} or GND, I_O=0mA				14	μA

Note: All typical values are for T_A = 25°C.

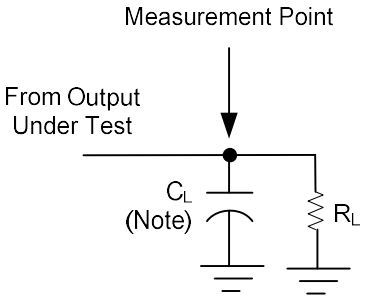
■ SWITCHING CHARACTERISTICS (T_A=-40~+125°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay	t_{pd}	V_{CCA}=1.80±0.15V	V_{CCB}=1.80±0.15V	0.5		20	ns
			V_{CCB}=2.50±0.20V	0.5		17	ns
			V_{CCB}=3.30±0.30V	0.5		14	ns
		V_{CCA}=2.50±0.20V	V_{CCB}=1.80±0.15V	0.5		18	ns
			V_{CCB}=2.50±0.20V	0.5		15	ns
			V_{CCB}=3.30±0.30V	0.5		12	ns
		V_{CCA}=3.30±0.30V	V_{CCB}=1.80±0.15V	0.5		16	ns
			V_{CCB}=2.50±0.20V	0.5		13	ns
			V_{CCB}=3.30±0.30V	0.5		10	ns

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Capacitance	C_I	V_{CCA}=3.3V, V_{CCB}=0V V_I=1.65V_{DC}+1MHz-16dBmsinewave			2		pF
Output Capacitance	C_O	V_{CCA}=0V, V_{CCB}=3.3V V_I=1.65V_{DC}+1MHz-16dBmsinewave			4		pF
Power Dissipation Capacitance -Port A	C_{PDA}	I_O=0mA, C_L=0pF, f=1MHz, t_r=t_f=1ns	V_{CCA}=V_{CCB}=1.8V		1		pF
			V_{CCA}=V_{CCB}=2.5V		1.3		pF
			V_{CCA}=V_{CCB}=3.3V		1.8		pF
Power Dissipation Capacitance -B Port	C_{PDB}	I_O=0mA, C_L=0pF, f=1MHz, t_r=t_f=1ns	V_{CCA}=V_{CCB}=1.8V		12		pF
			V_{CCA}=V_{CCB}=2.5V		15		pF
			V_{CCA}=V_{CCB}=3.3V		18		pF

■ TEST CIRCUIT AND WAVEFORMS

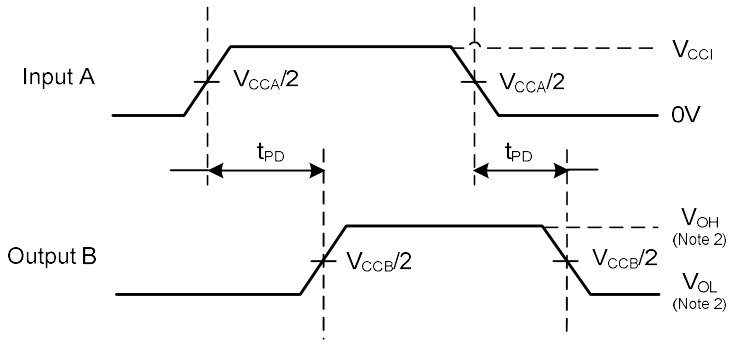


Load Circuit

TEST	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

Note: C_L includes probe and jig capacitance.

V_{CC}	C_L	R_L
1.65V ~3.6V	15pF	2KΩ



Propagation Delay Times

Notes: 1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified RL and C_L.

■ DETAILED DESCRIPTION

Overview

The **2N7001** is a single-bit dual-supply buffered voltage signal converter that can be used to up or downtranslate a single unidirectional signal. The device is operational with both V_{CCA} and V_{CCB} supplies down to 1.65V and up to 3.6V. V_{CCA} defines the input threshold voltage on the A input while V_{CCB} defines the output voltage on the B output.

■ FEATURES DESCRIPTION

Up-Translation or Down-Translation from 1.65V to 3.60V

The V_{CCA} and V_{CCB} pins can both be supplied by a voltage range from 1.65V to 3.6V. This voltage range makes the device suitable for translating between any of the voltage nodes (1.8V, 2.5V, and 3.3V).

Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent.

The electrical and thermal limits defined the in the Absolute Maximum Raings must be followed at all times.

Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance shown in the Electrical Characteristics. The worst case resistance is calculated with the maximum input voltage, shown in the Absolute Maximum Ratings, and the maximum input leakage current, shown in the Electrical Characteristics, using Ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in the Recommended Operating Conditions to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as shown in Figure 1.

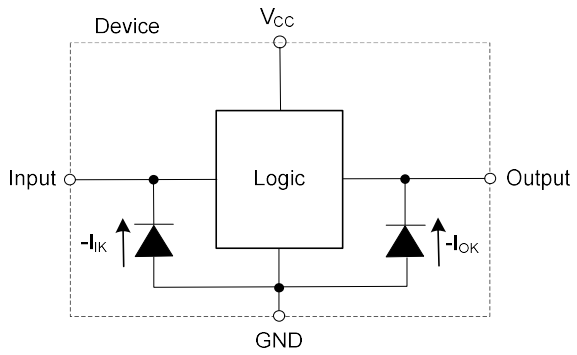


Figure 1. Electrical Placement of Clamping Diodes for Each Input and Output

Partial Power Down (Ioff)

The inputs and outputs for this device enter a high-impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input pin or output pin on the device is specified by Ioff in the Electrical Characteristics.

Over-voltage Tolerant Inputs

Input signals to this device can be driven above the input supply voltage (VCCA), as long as they remain below the maximum input voltage value specified in the Recommended Operating Conditions

■ TYPICAL APPLICATION CIRCUIT

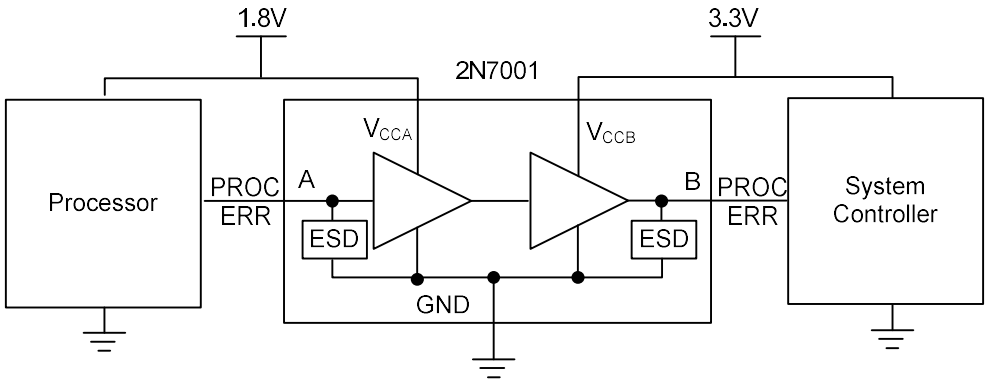


Figure 2. Processor Error Up Translation Application

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