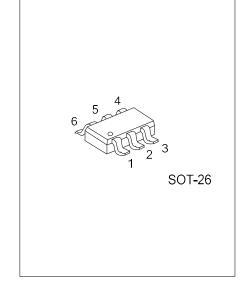
# ANALOG SWITCH, SPDT, $1\Omega RON$

#### DESCRIPTION

The UTC **UTAS4157** is a low R<sub>ON</sub> SPDT analog switch. This device is designed for low operating voltage, high current switching of speaker output for cell phone applications. It can switch a balanced stereo output. The UTC **UTAS4157** can handle a balanced microphone/speaker/ringtone generator in a monophone mode. The device contains a break-before-make (BBM) feature.

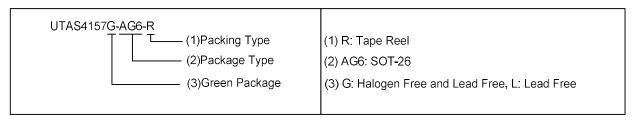


#### **■ FEATURES**

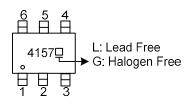
- \* Single Supply Operation: 1.65V to 5.5V V<sub>CC</sub> Function Directly from LiON Battery
- \* Low Static Power
- \*  $R_{ON}$  Typical = 0.9  $\Omega$  @  $V_{CC}$ = 4.5V

#### **■ ORDERING INFORMATION**

Ordering	Number	Dookogo	Docking
Lead Free	Halogen Free	Package	Packing
UTAS4157L-AG6-R	UTAS4157G-AG6-R	SOT-26	Tape Reel

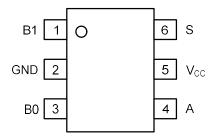


#### MARKING



<u>www.unisonic.com.tw</u> 1 of 8

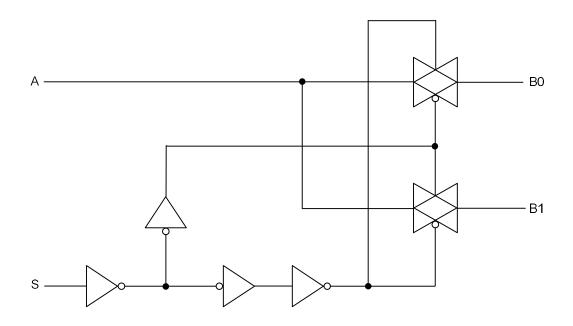
#### ■ PIN CONFIGURATION



## ■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1, 3, 4	B1, B0, A	Data Ports
2	GND	Ground
5	V <sub>CC</sub>	Power supply
6	S	Control Input

#### ■ INPUT EQUIVALENT CIRCUIT



# ■ TRUTH TABLE

CONTROL INPUT	FUNCTION
L	B0 Connected to A
Н	B1 Connected to A

#### ■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Positive DC Supply Voltage	V <sub>cc</sub>	-0.5 ~ +6.0	V
Analog Input Voltage (V <sub>NO</sub> , V <sub>NC</sub> , or V <sub>COM</sub> )	V <sub>IS</sub>	-0.5 ~ V <sub>CC</sub> +0.5	V
Digital Select Input Voltage	V <sub>IN</sub>	-0.5 ~ +6.0	\ \
Continuous DC Current from COM to NC/NO	I <sub>anl1</sub>	±300	mA
Peak Current from COM to NC/NO, 10 Duty Cycles (Note 2)	I <sub>anl-pk1</sub>	±500	mA
Continuous DC Current into COM/NC/NO with respect to V <sub>CC</sub> or GND	I <sub>clmp</sub>	±100	mA

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

#### ■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Positive DC Supply Voltage		V <sub>CC</sub>	1.65		5.5	V
Analog Input Voltage (A, B0, B1)		V <sub>IS</sub>	0		Vcc	V
Digital Select Input Voltage (S)		V <sub>IN</sub>	0		$V_{CC}$	V
Operating Temperature Range		T <sub>A</sub>	-40		+85	°C
Innut Bios on Fall Times CELECT	V <sub>CC</sub> =3.0V	t <sub>r</sub>			20	ns/V
Input Rise or Fall Time, SELECT	V <sub>CC</sub> =5.5V	t <sub>f</sub>			10	ns/V

<sup>2.</sup> Defined as 10% ON, 90% off duty cycle.

#### ■ DC ELECTRICAL CHARACTERISTICS

DADAMETED	CVMDOL	TEST COMPLETONS		T <sub>A</sub> =25°C			-40°C~+85°C		
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP MAX		MIN	TYP	MAX	UNIT
HIGH Level Input	.,	V <sub>CC</sub> =2.7V	2.0			2.0			V
Voltage	V <sub>IH</sub>	V <sub>CC</sub> =4.5V	2.4			2.4			
LOW Level Input	V <sub>IL</sub>	V <sub>CC</sub> =2.7V			0.6			0.6	V
Voltage	V IL	V <sub>CC</sub> =4.5V			0.8			0.8	
Input Leakage Current	I <sub>IN</sub>	V <sub>CC</sub> =0~5.5V, 0≤V <sub>IN</sub> ≤5.5 V			±0.1			±1	uA
OFF State Leakage Current (Note 6)	l <sub>OFF</sub>	V <sub>CC</sub> =5.5V, 0≤A, B≤V <sub>CC</sub>	-0.1		+0.1			±1	uA
ON State Leakage Current (Note 6)	I <sub>ON</sub>	V <sub>CC</sub> =5.5V, 0≤A, B≤V <sub>CC</sub>	-0.1		+0.1			±1	uA
Switch On Resistance (Note 1)  Ron  Ron  B <sub>0</sub> or B <sub>1</sub> = V <sub>CC</sub> =4.5\ B <sub>0</sub> or B <sub>1</sub> =		$V_{CC}$ =2.7V, $I_{O}$ = -100 mA, $B_{0}$ or $B_{1}$ =1.5V		3.9	6.0			6.3	Ω
	$V_{CC}$ =4.5V, $I_{O}$ = -100 mA, $B_{0}$ or $B_{1}$ =3.5V		0.9	2.0			2.3	Ω	
Quiescent Supply Current All Channels ON or OFF	Icc	$V_{CC}$ =5.5V, $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0			0.5			1.0	uA
ANALOG SIGNAL R	ANGE								
On Resistance Match Between	△Ron	V <sub>CC</sub> =2.7V, I <sub>A</sub> =-100mA, B <sub>0</sub> or B1=1.5V		0.15				0.15	Ω
Channels (Notes 1, 2, 3)	△ KON	V <sub>CC</sub> =4.5V, I <sub>A</sub> =-100mA, B <sub>0</sub> or B1=3.5V		0.12				0.15	Ω
On Resistance	Б	V <sub>CC</sub> =2.7V, I <sub>A</sub> =-100mA, B <sub>0</sub> or B1=0V, 0.75V, 1.5V		1.4				0.4	Ω
Flatness (Notes 1, 2, 4)	R <sub>flat</sub>	V <sub>CC</sub> =4.5V, I <sub>A</sub> =-100mA, B <sub>0</sub> or B1=0V, 1.0V, 2.0V		0.3				0.4	Ω

Notes: 1. Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

- 2. Parameter is characterized but not tested in production.
- 3.  $D_{RON} = R_{ON max} R_{ON min}$  measured at identical  $V_{CC}$ , temperature and voltage levels.
- 4. Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.
- 5. Guaranteed by Design.
- 6. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

#### ■ AC ELECTRICAL CHARACTERISTICS

PARAMETER	CVMBOL	TEST CONDITIONS		T <sub>A</sub> =25°C	;	-40°C~+85°C			LINIT
PARAMETER	SYMBOL	TEST CONDITIONS	MIN TYP		MAX	MIN	TYP	MAX	UNIT
Propagation Delay	t <sub>PHL</sub>	V <sub>CC</sub> =2.7V,V <sub>I</sub> =OPEN			2.0			2.2	ns
Bus to Bus (Note 1)	t <sub>PLH</sub>	V <sub>CC</sub> =4.5V			0.3			0.5	ns
Output Enable Time		$V_{CC}$ =2.7V, $B_0$ or B1=1.5V, $R_L$ =50 $\Omega$ , $C_L$ =35pF			60			70	ns
(B <sub>n</sub> to A)	t <sub>ON</sub>	$V_{CC}$ =4.5V, B <sub>0</sub> or B1=3.0V, R <sub>L</sub> =50 $\Omega$ , C <sub>L</sub> =35pF			50			60	ns
Output Disable Time		$V_{CC}$ =2.7V, B <sub>0</sub> or B1=1.5V, R <sub>L</sub> =50Ω, C <sub>L</sub> =35pF			20			25	ns
Turn ff Time (B Port to A Port)	I	$V_{CC}$ =4.5V, B <sub>0</sub> or B1=3.0V, R <sub>L</sub> =50Ω, C <sub>L</sub> =35pF			15			20	ns
Break Before Make	<b>t</b>	V <sub>CC</sub> =2.7V	0.5			0.5			ns
Time (Note 2)	t <sub>BBM</sub>	V <sub>CC</sub> =4.5V	0.5			0.5			ns
Charge Injection	Q	$C_L=1.0$ nF, $V_{GEN}=0$ V $V_{CC}=2.7$ V		26					рC
(Note 2)	ų ų	$R_{GEN}=0\Omega$ $V_{CC}=4.5V$		48					рC
Off Isolation (Note 3)	O <sub>IRR</sub>	V <sub>CC</sub> =2.7~5.5V, R <sub>L</sub> =50Ω, f=1.0MHz		-52					dB
Crosstalk	X <sub>talk</sub>	$V_{CC}$ =2.7~5.5V, $R_L$ =50 $\Omega$ , f=1.0MHz		-50					dB
−3 dB Bandwidth	BW	V <sub>CC</sub> =2.7~5.5V, R <sub>L</sub> =50Ω		40					MHz
Total Harmonic Distortion (Note 2)	THD	$V_{CC}$ =2.7~5.5V, R <sub>L</sub> =600Ω 0.5V <sub>P-P</sub> , f=20Hz to 20kHz		0.012					%

Notes: 1. Guaranteed by Design.

#### ■ **CAPACITANCE** (T<sub>A</sub>=25°C, unless otherwise specified)

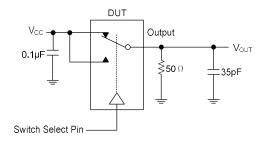
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Select Pin Input Capacitance	$C_{IN}$	V <sub>CC</sub> =0V, f=1MHz	10			pF
B Port Off Capacitance	$C_{IO-B}$	V <sub>CC</sub> =4.5V, f=1MHz	25			pF
A Port Capacitance when Switch is Enabled	C <sub>IOA-ON</sub>	V <sub>CC</sub> =4.5V, f=1MHz	87			pF

Note: f=1MHz, Capacitance is characterized but not tested in production.

<sup>2.</sup> This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

<sup>3.</sup> Off Isolation = 20 log10  $[V_A/V_{Bn}]$ .

#### **■ TYPICAL APPLICATION CIRCUIT**



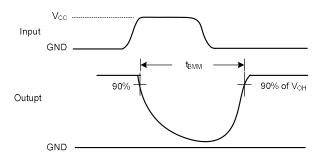
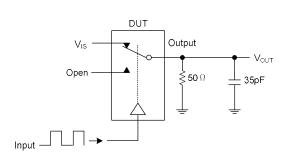


Figure 1. t<sub>BBM</sub> (Time Break-Before-Make)



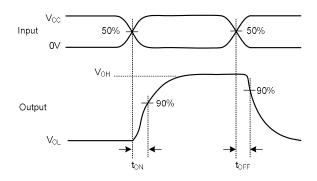
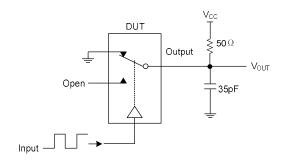


Figure 2. t<sub>ON</sub>/t<sub>OFF</sub>



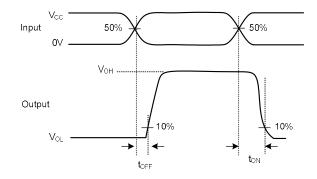
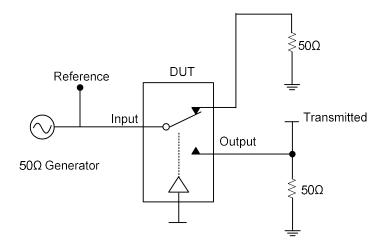


Figure 3. t<sub>ON</sub>/t<sub>OFF</sub>

## TYPICAL APPLICATION CIRCUIT (Cont.)



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch.  $V_{ISO}$ , Bandwidth and  $V_{ONL}$  are independent of the input signal direction.

$$V_{ISO}$$
 = Off Channel Isolation = 20 Log  $\frac{V_{OUT}}{V_{IN}}$  for  $V_{IN}$  at 100 kHz

$$V_{ONL}$$
 = On Channel Loss = 20 Log  $\frac{V_{OUT}}{V_{IN}}$  for  $V_{IN}$  at 100 kHz to 50 MHz

Bandwidth (BW) = the frequency 3 dB below V<sub>ONL</sub>

 $V_{CT}$  = Use  $V_{ISO}$  setup and test to all other switch analog input/outputs terminated with  $50\Omega$ 

Figure 4. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/VonL

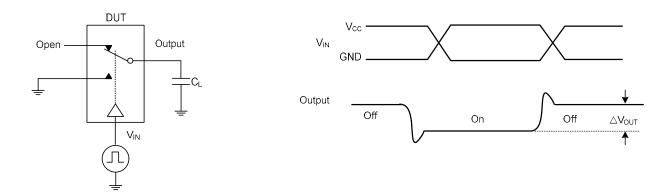
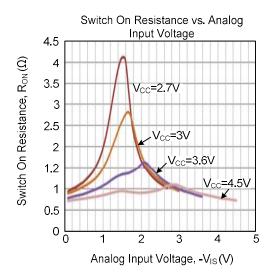


Figure 5. Charge Injection: (Q)

#### TYPICAL CHARACTERISTICS



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