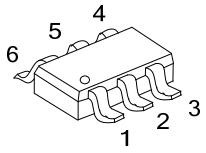
LOW COST POWER-SAVING MODE PWM CONTROLLER FOR FLYBACK CONVERTERS



SOT-26

■ DESCRIPTION

The UTC **UCQ3738** provides a CCM/valley switching mixed mode operation for better efficiency performance. The operation mode stays at CCM at heavy load, and switch to valley switching at light load.

The UTC **UCQ3738** is a high performance current mode PWM controller ideally suited for low standby power. Low V_{CC} startup current make the power reliable on startup design and a large value resistor could be used in the startup circuit to minimize the standby power. At no load condition, the IC operates in power-saving mode for lower standby power, decreasing frequency for Higher conversion efficiency at light load condition.

The UTC **UCQ3738** contains protection with automatic recovery including OLP (over load protection), OCP (cycle-by-cycle current limiting), and UVLO (V_{CC} over voltage clamp and under voltage lockout). It also provides the protections including OTP (over temperature protection), BNO(AC Brown Out protection) , LNO(AC Over voltage protection), Programmable Propagation Delay Time , OVP (V_{CC} or DC output over voltage protection) with automatic recovery. To protect the power MOSFET, Gate-drive output is fixed up to 16V max.

Leading-edge blanking on current sense input removes the signal glitch, which offering minima external component count in the design. Excellent EMI performance is achieved with UTC proprietary smart frequency hopping technique together with soft driver control. Audio noise is eliminated due to switch frequency more than 20kHz during operation.

UTC **UCQ3738** is packaged by using tiny SOT-26 package. It has such applications as: battery charger, power adaptor, set-top box power supplies, ink jet printers, open-frame SMPS.

■ FEATURES

* Proprietary smart frequency hopping for Improved EMI and output Jittering ripple
* Cycle-by-cycle current limiting
* CCM/Valley Switching Operation
* Fixed switch frequency 60~70kHz
* Dynamic peak current limiting for constant output power
* Programmable Propagation Delay Time
* Gate output voltage clamped at 16V
* Adjustable DC output OVP/UVP
* Adjustable OTP (Over Temperature Protection) on CS Pin
* OLP/V_{CC} OVP/OTP/BNO/LNO (automatic recovery)
* Internal Soft Start

■ ORDERING INFORMATION

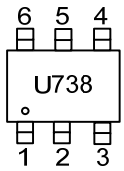
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UCQ3738L-AG6-R	UCQ3738G-AG6-R	SOT-26	Tape Reel

UCQ3738G-AG6-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) AG6: SOT-26 (3) G: Halogen Free and Lead Free, L: Lead Free

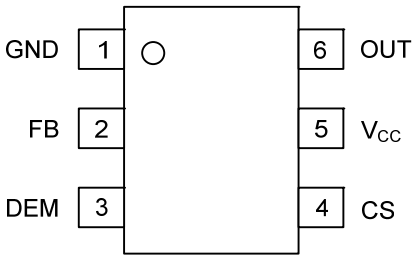
■ PROTECTION MODE

PRODUCT NAME	SWITCHING FREQ.	V_{CC}_OVP	FB_OVP	OSCP	OLP	BNI/BNO	CS_OTP	Int. OTP
UCQ3738	65kHz	Auto Recovery	Auto Recovery	Auto Recovery	Auto Recovery	Auto Recovery	Auto Recovery	Auto Recovery

■ MARKING



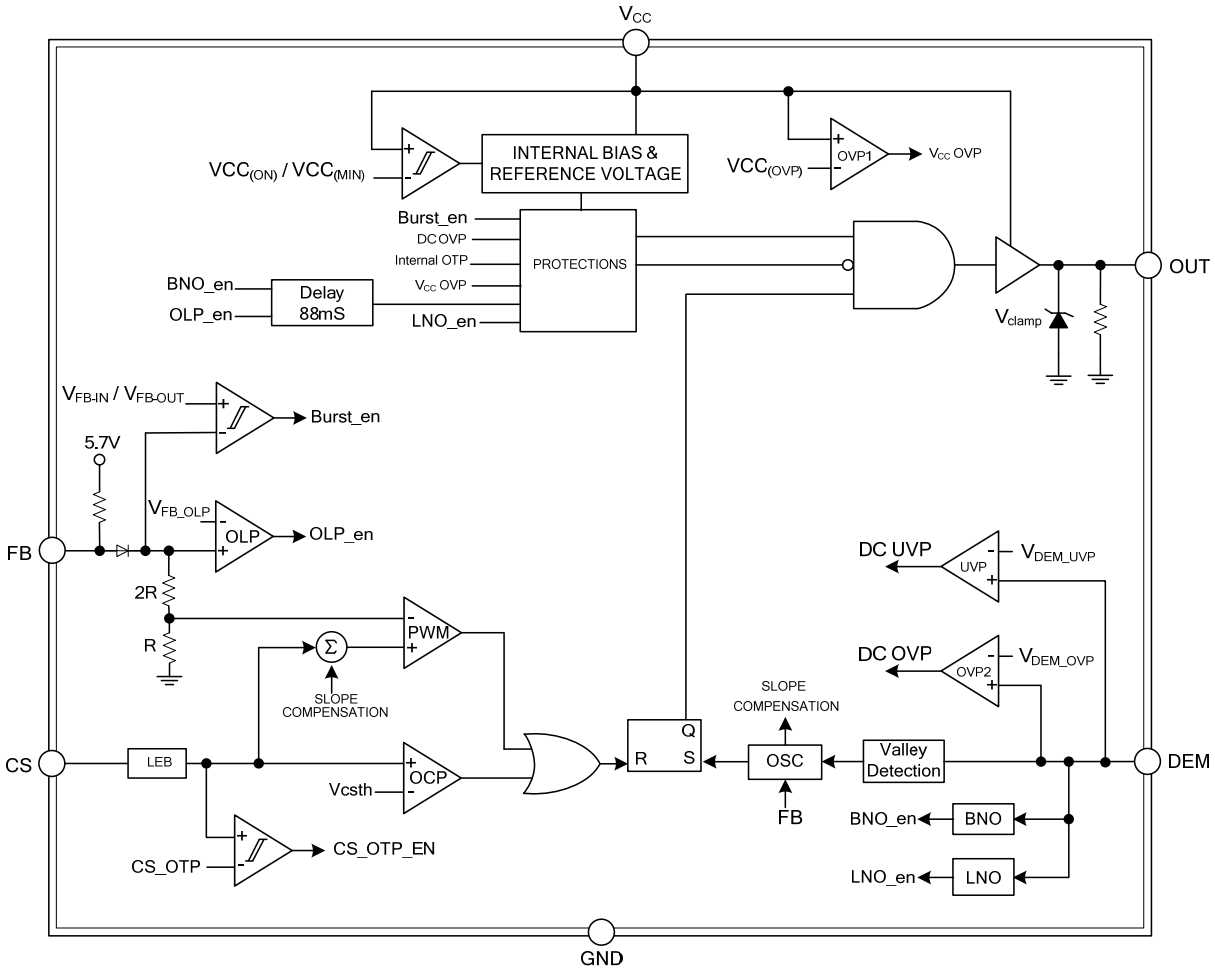
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground
2	FB	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and SENSE pin input
3	DEM	Demagnetization detection signal. This pin can also provide adjustable output voltage OVP and AC brown in/out protection
4	CS	Current sense input pin. Connected to MOSFET current sensing resistor node
5	V_{CC}	Power supply
6	OUT	The totem-pole output driver for driving the power MOSFET

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.3 ~ 32	V
Input Voltage to OUT Pin	V_{OUT}	-0.3 ~ V_{CC}+0.3	V
FB, CS, DEM		-0.3 ~ 6	V
Power Dissipation (T_A=25°C)	P_D	400	mW
Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_{OPR}	-40 ~ +85	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	9 ~ 30	V
Start up Resistor		0.86 ~ 4.4	MΩ
V_{CC} Capacitor		2.2 ~ 4.7	μF

■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	250	°C/W

■ ELECTRICAL CHARACTERISTICS (V_{CC}=15V, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{CC} (ON)	$V_{CC(ON)}$		14	15	16	V
V_{CC} (OFF)	$V_{CC(MIN)}$		6.6	7.6	8.6	V
Startup Current	I_{STR}	V_{CC}<$V_{CC(ON)}$-0.5V		1	5	μA
Operating Current	I_{OP}	V_{FB}=2.2V		1	2.5	mA
		V_{FB}=Burst Level		0.23		mA
V_{CC} OVP Threshold	$V_{CC(OVP)}$	V_{FB}=2.2V	30	32	34	V
OSCILLATOR & SWITCHING FREQUENCY						
Normal mode Switching Frequency	$F_{(SW)}$	V_{FB}=2.5V	60	65	70	KHz
Temperature Stability	F_{DT}	Guaranteed by Design			10	%
Voltage Stability	F_{DV}				10	%
Green Mode Frequency	$F_{(SW\_GR)}$		20	24		KHz
Frequency Spreading Range	ΔOSC	V_{FB}=2.2V	+9		-9	%
Max. Duty Cycle	DC_{MAX}	V_{FB}=2.2V, V_{CS}=0V	58	64	70	%
Internal Soft Start Time	T_{SS}	Guaranteed by Design		6		ms
VOLTAGE FEEDBACK						
Open Loop Voltage	V_{FB_Open}			3.3		V
OLP Level	V_{FB_OLP}			2.6		V
OLP De-Bounce Time	T_{D_OLP}	V_{FB}>5V	42	64	96	mS
Burst-Mode Enter FB Voltage	V_{FB-IN}			0.82		V
Burst-Mode Quit FB Voltage	V_{FB-OUT}			0.88		V
FB Pin Short Current	I_{FB_SHORT}			50		μA

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSING						
Current Limiting Threshold Voltage with 50% Duty	V_{CS_L}	V_{FB}=2.8V	0.36	0.4	0.44	V
Lead Edge Blanking Time	T_{LEB}	Guaranteed by Design		350		ns
SDSP(Secondary Diode Short Protection) CS pin Level	V_{SCP}	Guaranteed by Design	1.0	1.1	1.2	V
CS OTP Level	V_{CS_OTP}	Guaranteed by Design		0.7		V
Delay Time of External OTP	T_{D_OTP}	Guaranteed by Design	42	64	96	mS
GATE DRIVE OUTPUT						
Output Low Level	V_{OL}	V_{CC}=15V, I_{OUT}=-20mA			1	V
Output High Level	V_{OH}	V_{CC}=15V, I_{OUT}=20mA	9			V
Rising Time	t_R	10% to 90% of V_{OUT}, C_L=1nF		250		nS
Falling Time	t_F	90% to 10% of V_{OUT}, C_L=1nF		30		nS
Out Clamping	V_{clamp}	V_{CC}=20V		16		V
DEMAGNETIZATION (DEM) DETECTION						
DEM OVP Sampling Instant	T_{DEM_OVP1}	Guaranteed by Design		3		μS
DEM OVP Threshold Level	V_{DEM_OVP}		2.44	2.49	2.54	V
Output UVP Trigger Point	V_{DMAG_UVP}	Guaranteed by Design	0.36	0.4	0.44	V
DEM OVP De-Bounce Time	T_{DEM_OVP2}	Guaranteed by Design		7		Times
DEM_BNI	I_{BNI}	Guaranteed by Design		155		μA
DEM_BNO	I_{BNO}		120	130	140	μA
BNO De-Bounce Time	T_{BNO}	Guaranteed by Design		64		mS
Threshold Current of Line Voltage OVP	I_{LNO}			615		μA
THERMAL SHUT DOWN						
OTP Threshold	OTP			150		°C

■ APPLICATION NOTE

The UTC **UCQ3738** devices integrate many useful designs into one controller for low-power switch-mode power supplies. The following descriptions highlight some of the features of the UTC **UCQ3738** series.

Start-up Current

The start-up current is only 1μA. Low start-up current allows a start-up resistor with a high resistance and a low-wattage to supply the start-up power for the controller. For AC/DC adaptor with universal input range design, a 2.5~3MΩ, 1/8W startup resistor could be used together with a V_{CC} capacitor to provide a fast startup and low power dissipation solution. The D1 IN4148 can improve surge capability to 6.6KV.

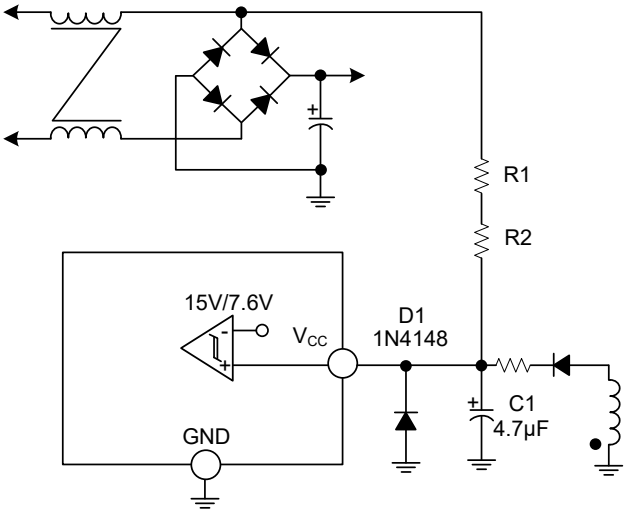


Fig. 1 Startup Circuit

Operation Mode

The UTC **UCQ3738** provides a CCM/valley switching mixed mode operation for better efficiency performance. The operation mode stays at CCM at heavy load, once if the converter enters into DCM, the UTC **UCQ3738** automatically finds the local minimum V_{DS} point and switching at this local valley.

Normally, the conduction loss is dominated at heavy load condition, and the switching loss turns to be larger than conduction loss in light load, especially at 1/4 ~ 1/2 of full load. By this kind of mixed mode operation to have CCM in heavy load and valley switching in light load can optimize the overall average efficiency during the entire operation range.

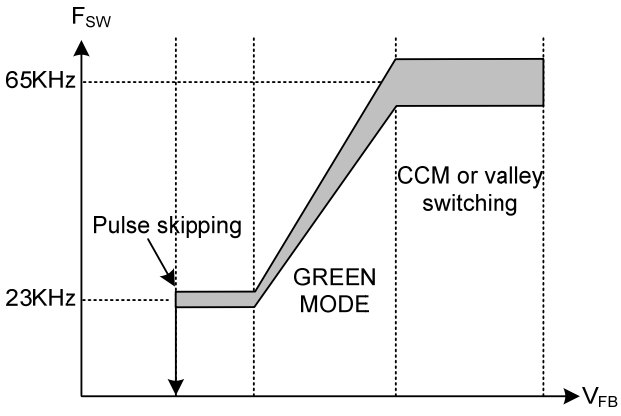


Fig. 2 Fosc vs V_{FB}

■ APPLICATION NOTE (Cont.)

As shown in Fig. 3, at deep light-load or no-load condition, the switching loss is the dominant factor. To improve the light-load efficiency, burst mode operation will stop the switching cycle of the OUT pin when FB pin voltage is below "V_{FB_IN}" Level and restart the switching cycle of the OUT pin when FB pin voltage is above "V_{FB_OUT}".

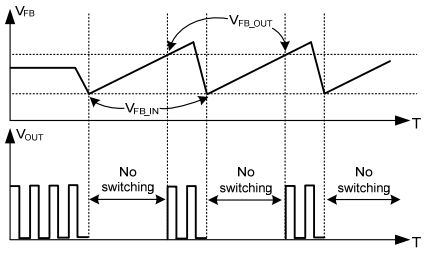


Fig. 3 Burst Mode Operation

Over Voltage Protection on V_{CC} Pin (V_{CC} OVP)

The V_{CC} OVP will shut down the switching of the power MOSFET whenever V_{CC} >V_{OVP}. The OVP event as followed Fig.4.

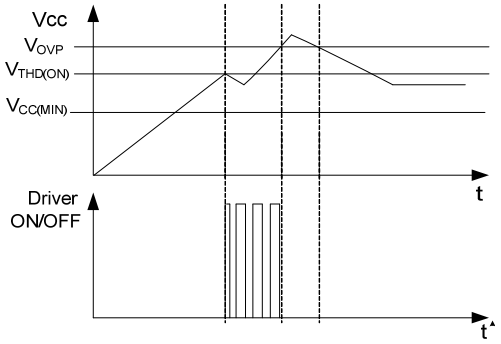


Fig.4 OVP case

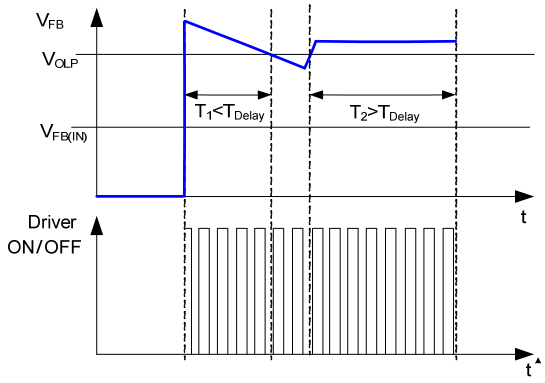


Fig.5 OLP case

Over Load &Open Loop & Output Short Protection (OLP or OSP)

OLP or OSP will shut down driver when V_{FB} > V_{OLP} for continual a blanking time. The OLP or OSP event as followed Fig.5.

Over Temperature Protection on CS pin (CS OTP)- Auto Recovery

UCQ3738 is implemented over temperature protection on CS pin which senses voltage to determine NTC status during gate off region. As VCS is greater than 0.7V and continues for 64ms, CS_OTP is triggered, than UCQ3738 is in auto recovery mode till the temperature drops to setting work condition.

Brown in/out and Line input OVP & DEM OVP/UVP Protection

To prevent high current stress at too low AC voltage condition, the UTC **UCQ3738** implements an AC brown in/out protection through the DEM pin. The current sourcing out from the DEM pin when the OUT pin is enabled is monitored to have the AC input voltage level information. When the current keeps above the DEM_BNI threshold (I_{BNI}) for more than BNI De-bounce time 7 cycles, the AC brown in condition is issued and the OUT is enabled. Once if the current keeps under the DEM_BNO threshold (I_{BNO}) for more than BNO De-bounce time, the AC brown out condition is issued and the OUT is disabled.

The equation is used to calculate the brown in/out level:

$$V_{AC\_BNI} = I_{BNI} \times \frac{R_{DEM\_U}}{\sqrt{2}} \times \frac{N_{PRI}}{N_{AUX}} \quad , \quad V_{AC\_BNO} = I_{BNO} \times \frac{R_{DEM\_U}}{\sqrt{2}} \times \frac{N_{PRI}}{N_{AUX}}$$

■ APPLICATION NOTE (Cont.)

To prevent line AC input voltage too high, the UTC **UCQ3738** implements an AC input LNO protection through the DEM pin. The current sourcing out from the DEM pin when the OUT pin is enabled is monitored to have the AC input voltage level information. When the current keeps above the DEM_LNO threshold (I_{LNO}) for more than LNO De-bounce time 7 cycles, AC input LNO protection is enabled and the out is off.

The equation is used to calculate the LNO level:

$$V_{AC\_LNO} = I_{LNO} \times \frac{R_{DEM\_U}}{\sqrt{2}} \times \frac{N_{PRI}}{N_{AUX}}$$

An over voltage protection for Vo is fulfilled by sampling the voltage on the DEM waveform after OUT is turn-off. After a short delay after OUT off, the sampled voltage is compared to the internal over voltage reference is determined whether if an OVP event is occurred. The internal over voltage reference is biased at V_{DEM_OVP}, uses can define the resistor divider ratio by the equation below based on the desired OVP level:

$$V_{O\_OVP} = V_{DEM\_OVP} \times \frac{R_{DEM\_U} + R_{DEM\_D}}{R_{DEM\_D}} \times \frac{N_{SEC}}{N_{AUX}}$$

An under voltage protection for Vo is fulfilled by sampling the voltage on the DEM waveform after OUT is turn-off. After a short delay after OUT off, the sampled voltage is compared to the internal under voltage reference is determined whether if an UVP event is occurred. The internal under voltage reference is biased at V_{DEM_UVP}, uses can define the resistor divider ratio by the equation below based on the desired UVP level:

$$V_{O\_UVP} = V_{DEM\_UVP} \times \frac{R_{DEM\_U} + R_{DEM\_D}}{R_{DEM\_D}} \times \frac{N_{SEC}}{N_{AUX}}$$

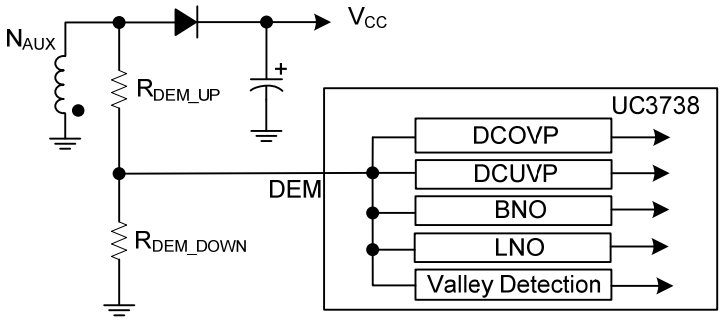


Fig. 6 DEM-Pin Divider

■ APPLICATION NOTE (Cont.)

Cycle by Cycle Over-Current Protection (OCP)

In a Flyback topology converter, the main MOSFET switch of the Flyback converter turns on and off rapidly. The energy is stored in the inductor when the MOSFET turns on. The inductor current flowing through the sensing resistor (R_{CS}) is shown in Fig.7. The current limit is determined by the equation below:

$$I_{PEAK} = \frac{V_{CS}}{R_{CS}}$$

In order to prevent the CS pin from false triggering, an internal leading edge blanking time (350nS Typ.) is added and an external low pass RC filter is also recommended to filter the turn-on spike of CS node.

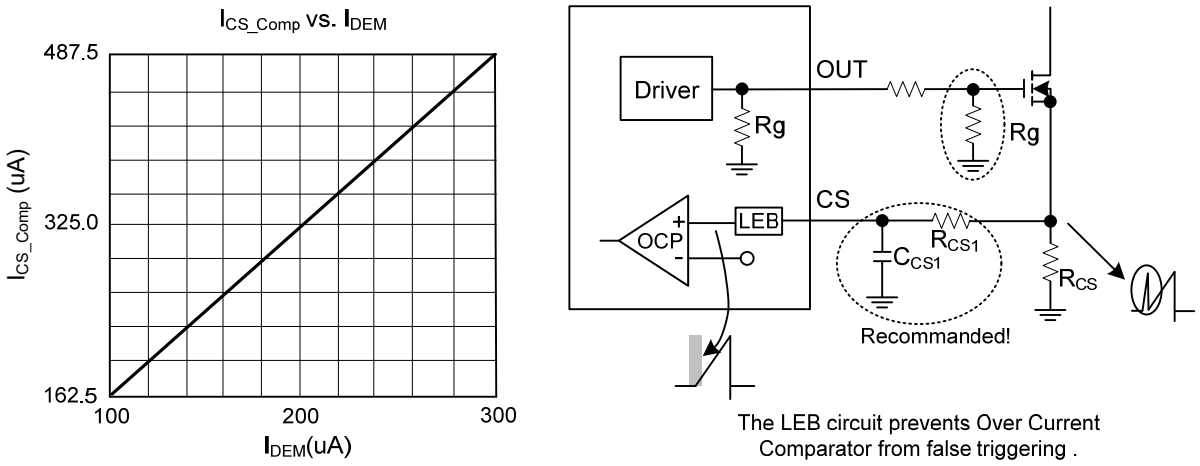


Fig. 7 Current Sensing

Programmable propagation delay time compensation

UCQ3738 provides programmable transmission delay time compensation. When the system switch turned on, the auxiliary winding voltage is negative at this time, and the **UCQ3738** voltage clamping circuit will output clamping current to clamp the demagnetization pin (DEM) voltage at zero voltage, and this clamping current is proportional to the input voltage.

UCQ3738 outputs the transmission delay compensation current through the gain ratio on the current sensing (CS) pin. The product R & D designer can compensate the transmission delay error caused by different output voltages by adjusting the transmission delay compensation resistance (RPDC), so as to achieve the purpose of maintaining the same output current and accurate overload protection under the high and low voltage input of the system.

At the beginning, the power engineer designed to set the initial transmission delay time compensation with an RPDC of 470 Ω and a CRC of 100pF, it is desirable to maintain the same output current under the high and low voltage input of the system, as shown in curve (1).The transmission delay time will vary with different high and low voltage inputs due to the different design of system components such as system transformer inductance, switch parasitic capacitance, switch gate series resistance, etc. If the overload protection curve is shown in curve (2), it can be adjusted by fine-tuning the RPDC resistance increase; If the overload protection curve is shown in curve (3), it can be adjusted by fine-tuning the increase of CRC capacity. The power engineer can adjust the RPDC and CRC to optimize the overload protection curve by setting the transmission delay time compensation, so that the overload protection curve can maintain the same output current under different high and low voltage inputs.

■ APPLICATION NOTE (Cont.)

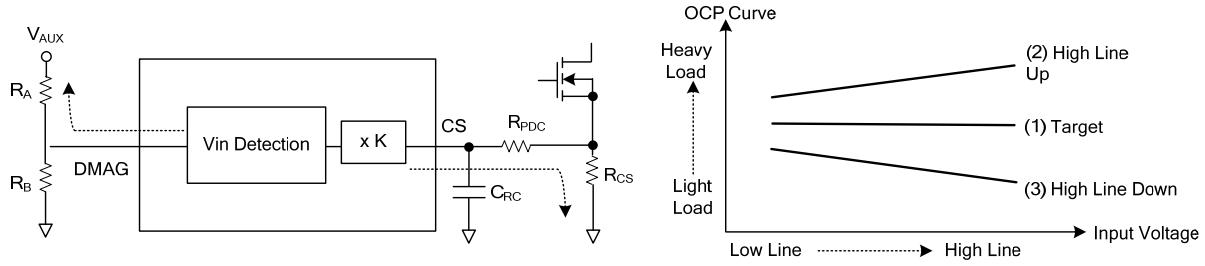


Figure 8. Diagram of Propagation Delay Time Compensation and OLP

■ TYPICAL APPLICATION CIRCUIT