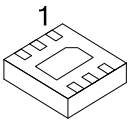
18V, 2A SYNC.STEP-DOWN CONVERTER



DFN2020-6

■ DESCRIPTION

The UTC **UD182012** is a monolithic buck switching regulators based on I2 architecture for fast transient response. Operating with an input range of 4.5V~18V, UTC **UD182012** delivers 2A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. At light loads, UTC **UD182012** operates in low frequency to maintain high efficiency.

UTC **UD182012** guarantees robustness with output short protection, thermal protection, current run-away protection and input under voltage lockout.

■ FEATURES

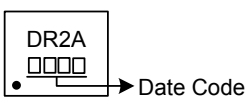
* 4.5V to 18V operating input range 2A output current
* Up to 95% efficiency
* PFM at light load
* 600kHz switching frequency
* Internal soft-start
* Input under-voltage lockout
* Current run-away protection
* Output short protection
* Thermal protection

■ ORDERING INFORMATION

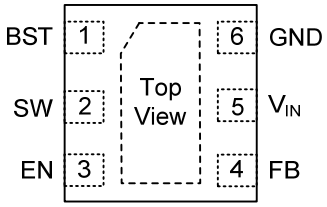
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UD182012L-K06-2020-R	UD182012G-K06-2020-R	DFN2020-6	Tape Reel

UD182012G-K06-2020-R (1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) K06-2020: DFN2020-6 (3) G: Halogen Free and Lead Free

■ MARKING



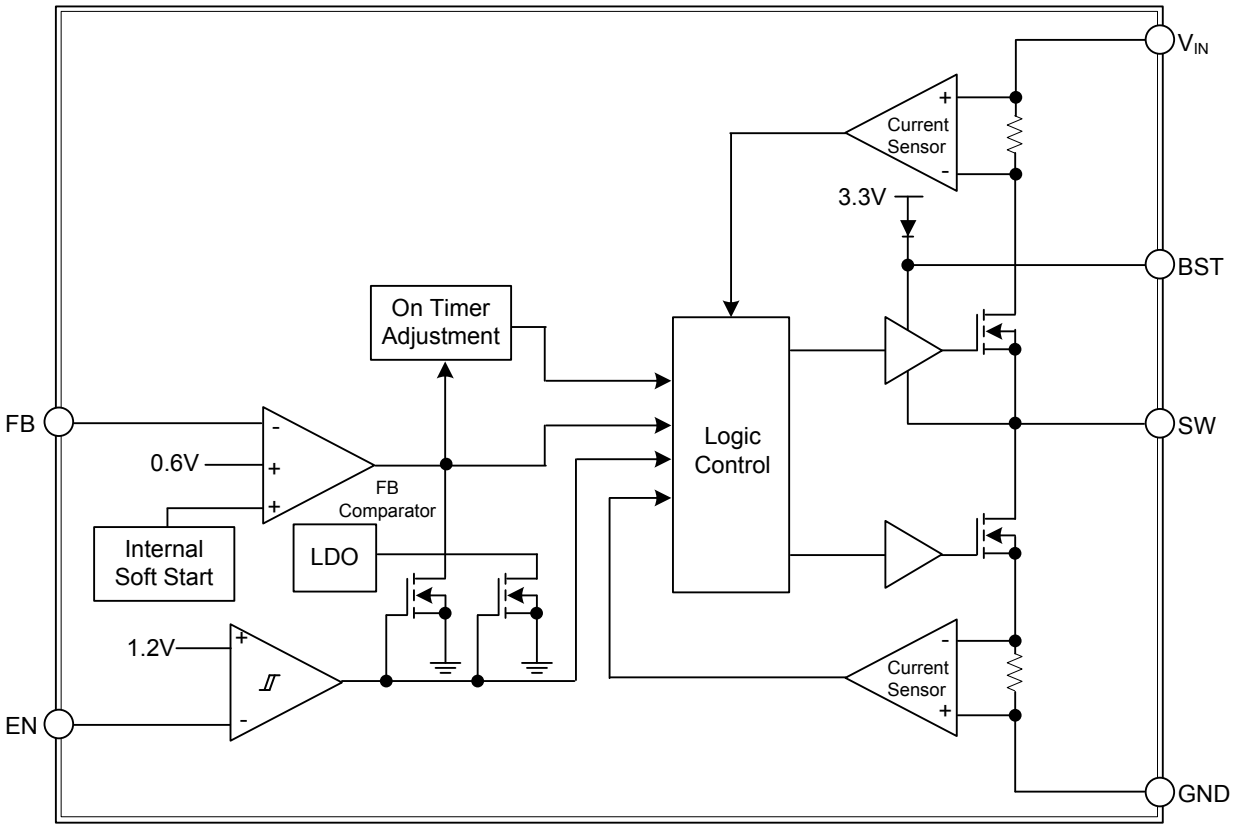
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	BST	Connect a 0.1μF capacitor between BST and SW pin to supply voltage for the top switch driver.
2	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
3	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
4	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6V. Connect a resistive divider at FB.
5	V_{IN}	Input voltage pin. VIN supplies power to the IC. Connect a 4.5V to 18V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
6	GND	Ground pin.
Exposed Pad	GND	Connect exposed pad to GND.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
V_{IN}, EN Pin		-0.3 ~ 20	V
SW Pin		-0.3V(-5V for 10ns) to 20V(22V for 10ns)	
BST Pin		SW-0.3V to SW+4V	
All other Pins		-0.3 ~ 4	V
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{STG}	-65 ~ +150	°C
RECOMMENDED OPERATING CONDITIONS			
Input Voltage	V_{IN}	4.5 ~ 18	V
Output Voltage	V_{OUT}	0.6~ V_{IN} × D_{MAX}	
Operation Junction Temperature	T_J	-40 ~ +125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

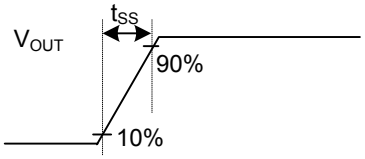
PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	θ_{JA}	75	°C/W
Junction to Case	θ_{JC}	20	°C/W

Note: Device mounted on FR-4 substrate P_C board, 2oz copper, with 1inch square copper plate.

■ ELECTRICAL CHARACTERISTICS (V_{IN}=12V, T_A=25°C, unless otherwise stated)

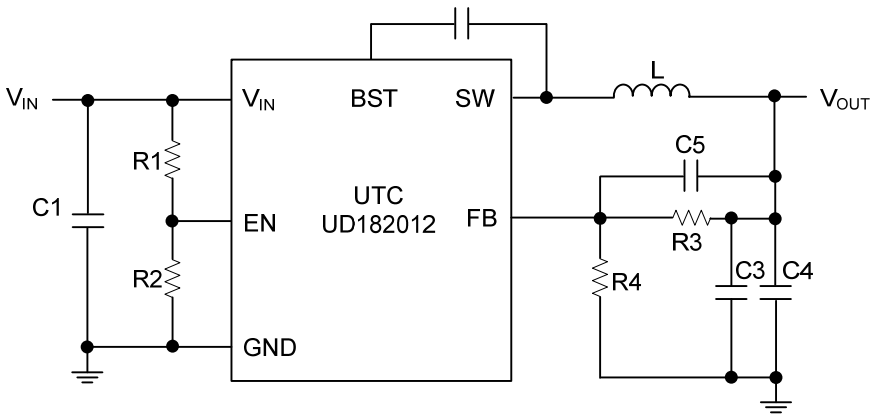
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} Under Voltage Lockout Threshold	V_{IN_MIN}	V_{IN} rising		4.2		V
V_{IN} Under voltage Lockout Hysteresis	$V_{IN\_MIN\_HYST}$			300		mV
Shutdown Supply Current	I_{SD}	V_{EN}=0V			1	μA
Supply Current	I_Q	V_{EN}=5V, V_{FB}=1V		140		μA
Feedback Voltage	V_{FB}	4.5V<V_{VIN}<18V		600		mV
FB Leakage Current	I_{FB}	V_{FB}=0.85V			100	nA
Top Switch Resistance	$R_{DS(ON)T}$			130		mΩ
Bottom Switch Resistance	$R_{DS(ON)B}$			70		mΩ
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=18V, V_{EN}=0V, V_{SW}=0V			1	μA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}=18, V_{EN}=0V, V_{SW}=18V			1	μA
Bottom Switch Current Limit	I_{LIM_BOT}			2.7		A
Minimum On Time (Note 1)	T_{ON_MIN}			120		ns
Minimum Off Time	T_{OFF_MIN}	V_{FB}=0.4V		150		ns
Maximum On Time	T_{ON_Max}			4		us
EN Rising Threshold	V_{EN_H}	V_{EN} rising		1.2		V
EN Falling Threshold	V_{EN_L}	V_{EN} falling		1.05		V
Soft-Start Period (Note 1, 2)	t_{SS}			1		ms
Frequency	f_{SW}			600		kHz
Thermal Shutdown (Note 1)	T_{TSD}			160		°C
Thermal Shutdown Hysteresis (Note 1)	T_{TSD_HYST}			20		°C

Notes: 1. Guaranteed by design.
2. Soft-Start Period is tested from 10% to 90% of the steady state output voltage.



t_{SS} Waveform

■ TYPICAL APPLICATION CIRCUIT



$$V_{FB}=V_{OUT}\times\frac{R4}{R4+R3}$$