

UNISONIC TECHNOLOGIES CO., LTD

UPG40N65

Preliminary

Insulated Gate Bipolar Transistor

# 650V, SMPS N-CHANNEL IGBT

# DESCRIPTION

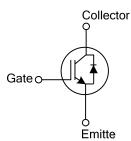
The UTC **UPG40N65** is a N-channel IGBT. it uses UTC's advanced technology to provide customers with high input impedance, high switching speed and low conduction loss, etc.

The UTC **UPG40N65** is suitable for high voltage switching, high frequency switch mode power supplies.

# FEATURES

- \*  $V_{CE(SAT)} \le 2.3V @ I_C=20A, V_{GE}=15V$
- \* High switching speed
- \* High input impedance
- \* Low conduction loss

# SYMBOL



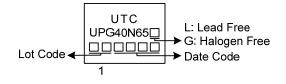
TO-247

### ORDERING INFORMATION

Ordering Number		Deelvere	Pin Assignment			Dealises	
Lead Free	Halogen Free	Package	1	2	3	Packing	
UPG40N65L-T47-T UPG40N65G-T47-T		TO-247	G	С	E	Tube	
Note: Pin Assignment: G: Gate C: Collector E: Emitter							
UPG40N65G-T47-T		(1) T: Tube					

	(T) acking Type	(1) 1. 1000
	(2)Package Type	(2) T47: TO-247
	(3)Green Package	(3) G: Halogen Free and Lead Free, L: Lead Free

### MARKING



#### ■ ABSOLUTE MAXIMUM RATINGS (T<sub>c</sub>=25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Collector-Emitter Voltage		V <sub>CES</sub>	650	V
Gate to Emitter Voltage Continuous		V <sub>GES</sub>	±20	V
	T <sub>C</sub> =25°C		80	А
Continuous Collector Current	T <sub>C</sub> =100°C	I <sub>C</sub>	40	А
Collector Current Pulsed (Note 2)		I <sub>CM</sub>	160	А
	T <sub>C</sub> =25°C		40	А
Continuous Forward Current	T <sub>C</sub> =100°C	I <sub>F</sub>	650 ±20 80 40 160	А
Forward Current Pulsed		I <sub>FM</sub>	140	А
Peak Diode Recovery dv/dt (Note 3)		dv/dt	6.2	V/ns
Power Dissipation		PD	242	W
Junction Temperature		TJ	-55 ~ +150	°C
Storage Temperature Range		T <sub>STG</sub>	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3.  $I_F \leq 9.0A$ , di/dt  $\leq 200A/\mu s$ ,  $V_{CC} \leq BV_{CES}$ , Starting  $T_J=25^{\circ}C$ 

#### THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Case	θ <sub>JC</sub>	0.51	°C/W

#### ELECTRICAL CHARACTERISTICS (T<sub>J</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Collector-Emitter Breakdown Voltage	<b>BV</b> <sub>CES</sub>	I <sub>C</sub> =250μA, V <sub>GE</sub> =0V		650			V
Collector-Emitter Leakage Current	I <sub>CES</sub>	V <sub>CE</sub> =650V, V <sub>GE</sub> =0V				10	μA
Gate to Emitter Leakage Current	I <sub>GES</sub>	V <sub>CE</sub> =0V, V <sub>GE</sub> =±20V				±400	nA
ON CHARACTERISTICS							
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	I <sub>C</sub> =250µA, V <sub>CE</sub> =V <sub>GE</sub>		4.0		6.0	V
			TJ=25°C		1.9	2.3	V
Collector-Emitter Saturation Voltage	V <sub>CE(SAT)</sub>	I <sub>C</sub> =40A, V <sub>GE</sub> =15V	Т <sub>Ј</sub> =150°С		2.2		V
DYNAMIC CHARACTERISTICS							
Input Capacitance	CIES	V <sub>CE</sub> =25V, V <sub>GE</sub> =0V, f=1MHz			2950		pF
Output Capacitance	COES				315		pF
Reverse Transfer Capacitance	C <sub>RES</sub>				58		pF
SWITCHING CHARACTERISTICS							
Total Gate Charge	$Q_{G}$	I <sub>C</sub> =40A, V <sub>CE</sub> =100V, V <sub>GE</sub> =10V			122		nC
Gate-Emitter Charge	$Q_GE$				26		nC
Gate-Collector Charge	Q <sub>GC</sub>				43		nC
Current Turn-On Delay Time	t <sub>D(ON)</sub>				19		ns
Current Rise Time	t <sub>R</sub>	I <sub>C</sub> =40A, V <sub>CE</sub> =100V, V <sub>GE</sub>	=15V,		24		ns
Current Turn-Off Delay Time	t <sub>D(OFF)</sub>	$R_{G}=10\Omega$			135		ns
Current Fall Time	t <sub>F</sub>	1			65		ns
DRAIN-SOURCE DIODE CHARACTER	ISTICS						
Forward Voltage Drop	V <sub>FM</sub>	I <sub>F</sub> =40A			2.1		V
Reverse Recovery Time	t <sub>rr</sub>				106		ns
Reverse Recovery Charge	Q <sub>rr</sub>	−I <sub>F</sub> =30A, dI/dt=100A/μS, V <sub>CC</sub> =400V			168		nC

Note: Pulse Test: Pulse width  ${\leq}\,50\mu s.$ 



# ■ TEST CIRCUIT AND WAVEFORMS

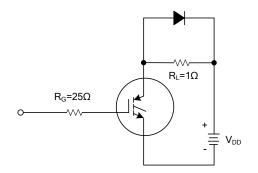


Fig 1. INDUCTIVE SWITCHING TEST CIRCUIT

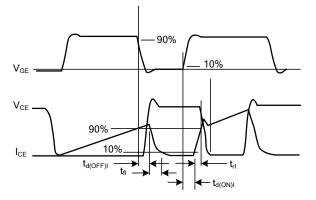


Fig 2. SWITCHING TEST WAVEFORMS

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