



U74AHC541

CMOS IC

OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

DESCRIPTION

The **U74AHC541** is a octal buffers/drivers with 3-state outputs and 8 channels.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FEATURES

- * Operate from 2V to 5.5V
- * Balanced propagation delays
- * Inputs accepts voltages higher than V_{CC}

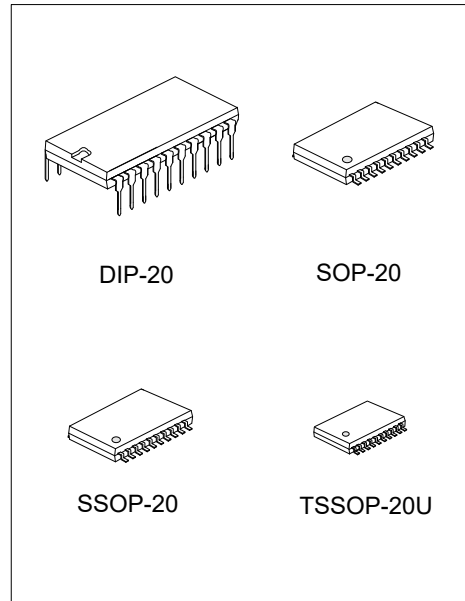
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHC541L-D20-T	U74AHC541G-D20-T	DIP-20	Tube
U74AHC541L-S20-R	U74AHC541G-S20-R	SOP-20	Tape Reel
U74AHC541L-R20-R	U74AHC541G-R20-R	SSOP-20	Tape Reel
U74AHC541L-ULA-R	U74AHC541G-ULA-R	TSSOP-20U	Tape Reel

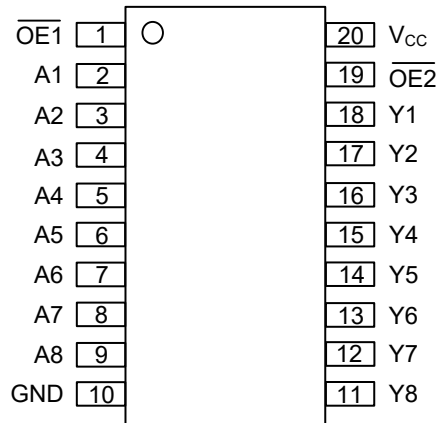
<p>U74AHC541G-D20-T</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Green Package 	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) D20: DIP-20, S20: SOP-20, R20: SSOP-20</p> <p>ULA: TSSOP-20U</p> <p>(3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

DIP-20	SOP-20 / SSOP-20 / TSSOP-20U
<p>Pin numbers 20 to 11 are shown above the chip, and 1 to 10 below. Marking locations are indicated by arrows: Date Code (pins 11-14), L: Lead Free (pin 12), G: Halogen Free (pin 13), Lot Code (pins 14-17).</p>	<p>Pin numbers 20 to 11 are shown above the chip, and 1 to 10 below. Marking locations are indicated by arrows: Date Code (pins 11-14), L: Lead Free (pin 12), G: Halogen Free (pin 13), Lot Code (pins 14-17).</p>



■ PIN CONFIGURATION

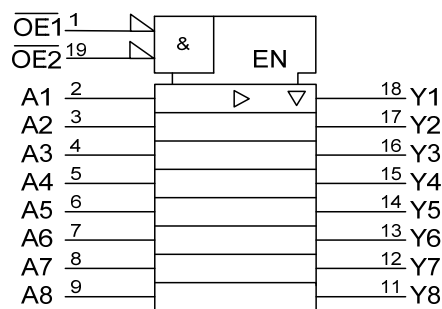


■ FUNCTION TABLE

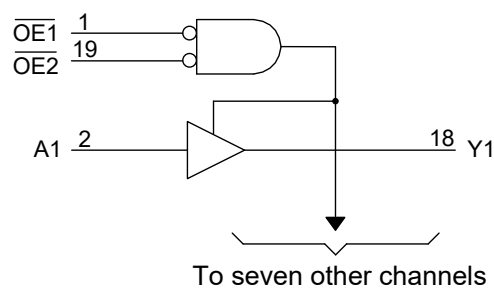
INPUTS $\overline{OE1}$	INPUTS $\overline{OE2}$	INPUTS(A)	OUTPUT(Y)
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = High voltage level ; L = Low voltage level ; X = Don't care

■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V _{CC}		-0.5 ~ 7	V
Input Voltage	V _{IN}	V _{OUT} <0 or V _{OUT} >V _{CC}	-0.5 ~ 7	V
Output Voltage	V _{OUT}		-0.5 ~ V _{CC} +0.5	V
Continuous current through V _{CC} or GND	I _{CC}		±75	mA
Continuous Output Current	I _{OUT}	V _{OUT} <0 or V _{CC}	±25	mA
Input Clamp Current	I _{IK}	V _{IN} <0	-20	mA
Output Clamp Current	I _{OK}	V _{OUT} <0 or V _{OUT} >V _{CC}	±20	mA
Storage Temperature	T _{STG}		-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage	V _{CC}		2		5.5	2		5.5	V
High-Level Input Voltage	V _{IH}	V _{CC} =2V	1.5			1.5			V
		V _{CC} =3V	2.1			2.1			
		V _{CC} =5.5V	3.85			3.85			
Low-Level Input Voltage	V _{IL}	V _{CC} =2V			0.5			0.5	V
		V _{CC} =3V			0.9			0.9	
		V _{CC} =5.5V			1.65			1.65	
Input Voltage	V _{IN}		0		5.5	0		5.5	V
Output Voltage	V _{OUT}		0		V _{CC}	0		V _{CC}	V
Input Transition Rise or Fall Rate	Δt/ΔV	V _{CC} =3.3V±0.3V			100			100	ns/V
		V _{CC} =5V±0.5V			20			20	
Operating Temperature	T _A		-40		+125	-40		+125	°C

Note: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-20	90	°C/W
	SOP-20	115	°C/W
	SSOP-20	130	°C/W
	TSSOP-20U	135	°C/W

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
High-Level Output Voltage	V _{OH}	V _{CC} =2V, I _{OH} =-50μA	1.9			1.9			V
		V _{CC} =3V, I _{OH} =-50μA	2.9			2.9			V
		V _{CC} =4.5V, I _{OH} =-50μA	4.4			4.4			V
		V _{CC} =3V, I _{OH} =-4mA	2.58			2.40			V
		V _{CC} =4.5V, I _{OH} =-8mA	3.94			3.70			V
Low-Level Output Voltage	V _{OL}	V _{CC} =2V, I _{OL} =50μA			0.1			0.1	V
		V _{CC} =3V, I _{OL} =50μA			0.1			0.1	V
		V _{CC} =4.5V, I _{OL} =50μA			0.1			0.1	V
		V _{CC} =3V, I _{OL} =4mA			0.36			0.55	V
		V _{CC} =4.5V, I _{OL} =8mA			0.36			0.55	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =0~5.5V, V _{IN} =5.5V or GND			±0.1			±2.0	μA
Output Off-state Current	I _{oz}	V _{CC} =5.5V, V _{IN} (\overline{OE})=V _{IL} or V _{IH} , V _{OUT} =V _{CC} or GND			±0.25			±10	μA
Quiescent Supply Current	I _q	V _{CC} =5.5V, V _{IN} =V _{CC} or GND, I _{OUT} =0A			4			80	μA

■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	T _A =25°C			T _A =-40~+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation delay from input (A) to output (Y)	t _{PLH} / t _{PHL}	V _{CC} =3.3V±0.3V	C _L =15pF	5.0	8.0	1.0		9.0	ns
			C _L =50pF	7.5	11.5	1.0		13.5	ns
		V _{CC} =5V±0.5V	C _L =15pF	3.5	5.0	1.0		6.5	ns
			C _L =50pF	5.0	8.0	1.0		9.0	ns
Propagation delay from input (\overline{OE}) to output (Y)	t _{PZL} / t _{PZH}	V _{CC} =3.3V±0.3V	C _L =15pF	6.0	11.5	1.0		13.5	ns
			C _L =50pF	8.0	14	1.0		17.5	ns
		V _{CC} =5V±0.5V	C _L =15pF	4.7	7.2	1.0		9.0	ns
			C _L =50pF	6.2	9.2	1.0		11.5	ns
Output Disable Time From (A) to output (Y)	t _{PLZ} / t _{PHZ}	V _{CC} =3.3V±0.3V	C _L =15pF	7.0	11	1.0		14	ns
			C _L =50pF	9.0	15.5	1.0		19.5	ns
		V _{CC} =5V±0.5V	C _L =15pF	5.0	7.5	1.0		9.5	ns
			C _L =50pF	6.0	8.8	1.0		11	ns
Output Skew Time	t _{sk(O)}	V _{CC} =3.3V±0.3V			1.5			1.5	ns
		V _{CC} =5V±0.5V			1.0			1.0	ns

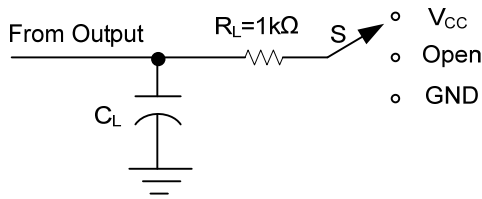
■ SWITCHING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiet output, maximum dynamic V _{OL}	V _{OL(P)}				0.8	V
Quiet output, minimum dynamic V _{OL}	V _{OL(V)}				-0.8	V
Quiet output, minimum dynamic V _{OH}	V _{OH(V)}		4.7			V
High-level dynamic input voltage	V _{IH(D)}		3.5			V
Low-level dynamic input voltage	V _{IL(D)}				1.5	V

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Capacitance	C _{IN}	V _{CC} =5.5V, V _{IN} =V _{CC} or GND		2	10	pF
Output Capacitance	C _{OUT}	V _{CC} =5.5V, V _{OUT} =V _{CC} or GND		4		pF
Power Dissipation Capacitance per flip-flop	C _{PD}	V _{CC} =5V, f=1MHz, No load.		12		pF

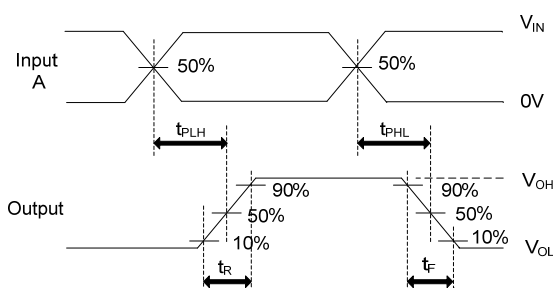
TEST CIRCUIT AND WAVEFORMS



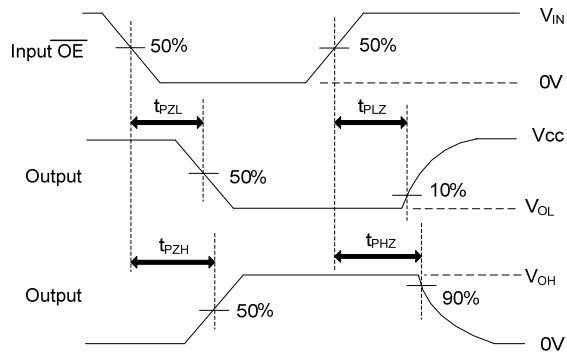
TEST CIRCUIT

TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{CC}

Parameter		R_L	C_L
t_{en}	t_{PZH}	1KΩ	15 pF or 50 pF
	t_{PZL}		
t_{dis}	t_{PZH}	1KΩ	15 pF or 50 pF
	t_{PZL}		
t_{PD} or t_t			15 pF or 50 pF



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{MHz}$, $Z_o = 50\Omega$,

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