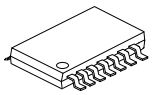
4-BITS BIDIRECTIONAL MULTI-VOLTAGE LEVEL TRANSLATOR FOR OPEN-DRAIN AND PUSH-PULL APPLICATION



TSSOP-14

■ DESCRIPTION

UTC **ULSF0204/D** family consists of bidirectional voltage level translators that operate from 0.8Vto 4.5V (V_{REF_A}) and1.8V to 5.5V (V_{REF_B}). This range allows for bidirectional voltage translations between 0.8V and 5.0V without the need for a direction terminal in open-drain or push-pull applications. The UTC **ULSF0204/D** family supports level translation applications with transmission speeds greater than 100MHz for open-drain systems that utilize a 15-pFcapacitance and 165Ω pull-up resistor.

When the An or Bn port is LOW, the switch is in the ON-state and a low resistance connection exists between the An and Bn ports. The low Ron of the switch allows connections to be made with minimal propagation delay and signal distortion. The voltage on the A or B side will be limited to V_{REF_A} and can be pulled up to any level between V_{REF_A} and 5V. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control.

■ FEATURES

* Provides bidirectional voltage translation with no direction pin
* Supports up to 100-MHz up translation and greater than 100MHz down translation at ≤ 30pF capacitor load and up to 40MHz up/down translation at 50pF capacitor load
* Supports I_{OFF}, partial power down mode
* Allow bidirectional voltage level translation between
  - 0.8V↔1.8/2.5/3.3/5V
  - 1.2V↔1.8/2.5/3.3/5V
  - 1.8V↔2.5/3.3/5V
  - 2.5V↔3.3/5V
  - 3.3V↔5V

■ ORDERING INFORMATION

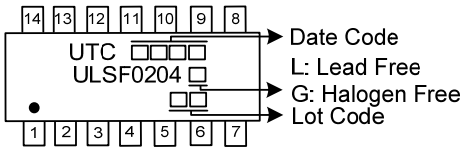
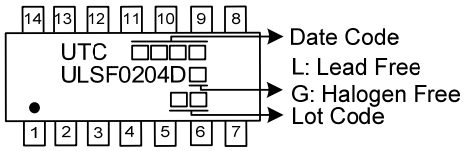
Ordering Number		Package	Packing
Lead Free	Halogen Free		
ULSF0204L-P14-R	ULSF0204G-P14-R	TSSOP-14	Tape Reel
ULSF0204DL-P14-R	ULSF0204DG-P14-R	TSSOP-14	Tape Reel

ULSF0204DG-P14-R

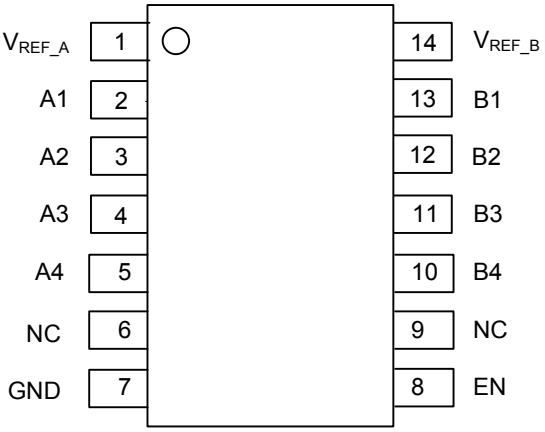
(1)Packing Type
(2)Package Type
(3)Green Package
(4)Logic Level

(1) R: Tape Reel
(2) P14: TSSOP-14
(3) G: Halogen Free and Lead Free, L: Lead Free
(4) Blank: EN is high-active, D: EN is low-active

■ MARKING

ULSF0204	ULSF0204D
	

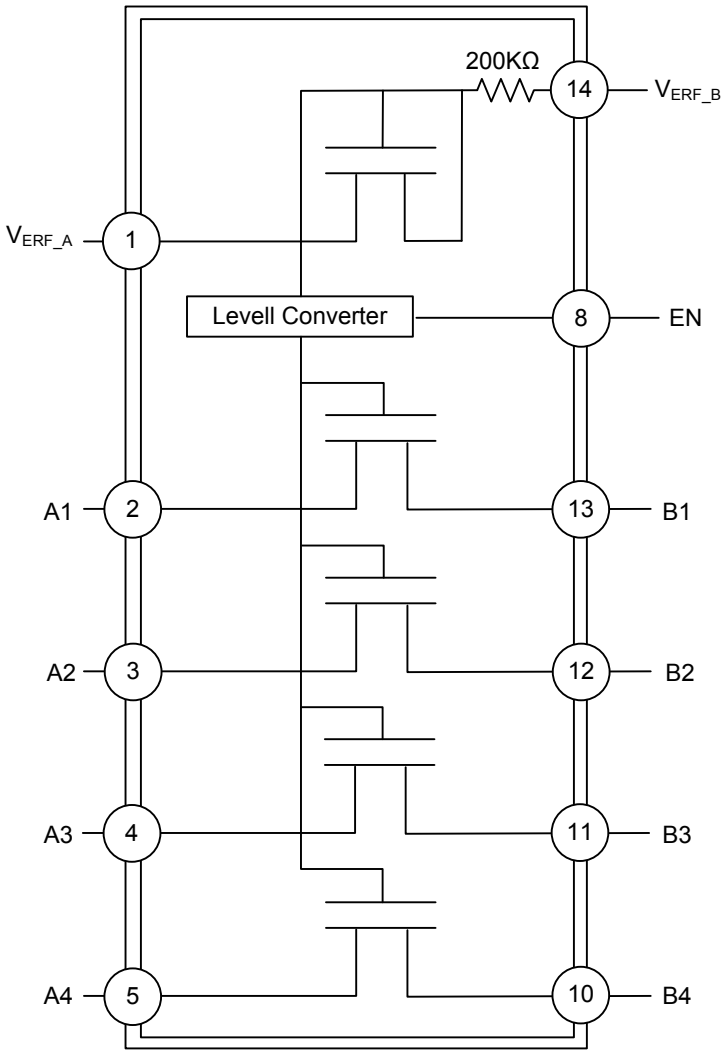
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{REF}_A	Reference supply voltage
2 ~ 5	An	Data port
6, 9	NC	No connection
7	GND	Ground
8	EN	Switch enable input **ULSF0204**: EN is high-active ; **ULSF0204D**: EN is low-active
10 ~ 13	Bn	Data port
14	V_{REF}_B	Reference supply voltage

■ BLOCK DIAGRAM



■ FUNCTION TABLE

PART NUMBER	INPUT EN PIN	FUNCTION
LSF0204	H	An = Bn
	L	Hi-Z
LSF0204D	H	Hi-Z
	L	An = Bn

Note: EN is controlled by V_{REF_A} logic levels.

■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Input Voltage (Note 3)	V_{IN}		-0.5 ~ 7	V
Input/output Voltage (Note 3)	$V_{I/o}$		-0.5 ~ 7	V
Continuous channel current			128	mA
Input Clamp Current		V_{IN}<0V	-50	mA
Junction temperature	T_J		+150	°C
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

■ REOMMENDED OPRATION CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input/output Voltage	$V_{I/O}$		0		5.5	V
Reference Voltage	$V_{REF\_A/B/EN}$		0		5.5	V
Pass transistor current	I_{PASS}				64	mA
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP (Note 1)	MAX	UNIT
Input clamp Voltage	V_{IK}	I_I=-18mA,V_{EN}=0				-1.2	V
Input Leakage Current	I_{IH}	V_{IN}=5V,V_{EN}=0				5	μA
Leakage Current from B to A	I_{CC}	V_{REF_B}=3.3V, V_{REF_A}=V_{EN}=1.8V, I_O=0, V_I=3.3V or GND				3.5	μA
Total Current through GND (Note 4)	I_{CCA}+I_{CCB}	V_{REF_B}=3.3V, V_{REF_A}=V_{EN}=1.8V, I_O=0, V_I=3.3V or GND			0.2		μA
Control pin current	I_{IN}	V_{REF_B}=5.5V, V_{REF_A}=4.5V, I_O=0, V_{EN}=0 to V_{REF_A}				±1	μA
Power off Leakage current	I_{OFF}	V_{REF_B}= V_{REF_A} =0, V_{EN}=GND, I_O=0, V_I=5 or GND				±1	μA
Input Capacitance	C_{IN}	V_I=3V or 0			7.0		pF
Off Capacitance	$C_{IO(OFF)}$	V_O=3V or 0, V_{EN}=0			5.0	6.0	pF
Capacitance When Switch Is Enabled	$C_{IO(ON)}$	V_O=3V or 0, V_{EN}= V_{REF_A}			10.5	13	pF
High-Level Input Voltage for EN Pin (Note 3)	V_{IH}	V_{REF_A}=1.0V~1.5V		0.8× V_{REF_A}			V
High-Level Input Voltage for EN Pin		V_{REF_A}=1.5V~4.5V		0.7× V_{REF_A}			V
Low-Level Input Voltage for EN Pin	V_{IL}	V_{REF_A}=1.0V~1.5V				0.3× V_{REF_A}	V
		V_{REF_A}=1.5V~4.5V				0.3× V_{REF_A}	V
Input Transition Rise or Fall Rate for EN Pin	Δt/Δv				10		ns/V
Switch On Resistance (Note 2)	R_{ON}	V_I=0V, I_O=64mA	V_{REF_A}=V_{EN}=3.3V, V_{REF_B}=5V		3		Ω
			V_{REF_A}=V_{EN}=1.8V, V_{REF_B}=5V		4		Ω
		V_I=0V, I_O=32mA	V_{REF_A}=V_{EN}=1.0V, V_{REF_B}=5V		9		Ω
			V_{REF_A}=V_{EN}=1.8V, V_{REF_B}=5V		4		Ω
			V_{REF_A}=V_{EN}=2.5V, V_{REF_B}=5V		10		Ω
		V_I=1.8V, I_O=15mA	V_{REF_A}=V_{EN}=5V, V_{REF_B}=3.3V		5		Ω
		V_I=1V, I_O=10mA	V_{REF_A}=V_{EN}=3.3V, V_{REF_B}=1.8V		8		Ω
		V_I=0, I_O=10mA	V_{REF_A}=V_{EN}=3.3V, V_{REF_B}=1.0V		6		Ω
		V_I=0, I_O=10mA	V_{REF_A}=V_{EN}=1.8V, V_{REF_B}=1.0V		6		Ω

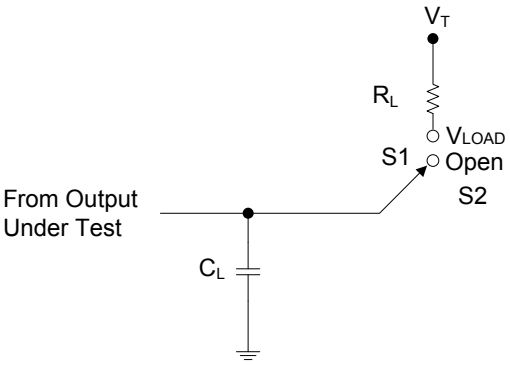
Notes: 1. All typical values are at T_A=25°C.

2. Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.
3. Enable pin test conditions are for the **ULSF0204**. The enable pin test conditions for **ULSF0204D** are oppositely set.
4. The actual supply current for **ULSF0204** is I_{CCA} + I_{CCB}, the leakage from V_{REF_B} to V_{REF_A} can be measured on V_{REF_A} and V_{REF_B} pin.

■ SWITCHING CHARACTERISTICS

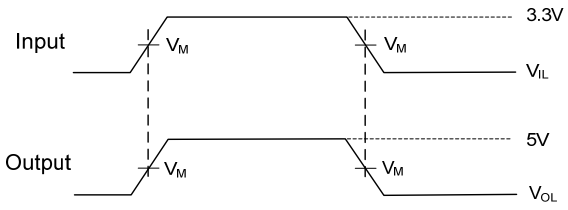
PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay From Input (A or B) to Output (B or A)	Down	t_{PLH}	V_{REF_A}=1.8V, V_{REF_B}=3.3V, V_{EN}=1.8V, R_L=NA, V_{IH}=3.3V, V_{IL}=0, V_M=1.15V	C_L=50pF		3.8	5.49	ns
				C_L=15pF		1.9	5.19	ns
			V_{REF_A}=1.2V, V_{REF_B}=3.3V, V_{EN}=1.2V, R_L=NA, V_{IH}=3.3V, V_{IL}=0, V_M=0.85V	C_L=50pF		2.1	4.1	ns
				C_L=15pF		2.2	3.8	ns
	Up		V_{REF_A}=1.8V, V_{REF_B}=3.3V, V_{EN}=1.8V, R_L=500Ω, V_{IH}=1.8V, V_{IL}=0, V_M=0.9V	C_L=50pF		2.3	5.7	ns
				C_L=15pF		1.9	5.13	ns
			V_{REF_A}=1.2V, V_{REF_B}=1.8V, V_{EN}=1.2V, R_L=500Ω, V_{IH}=1.2V, V_{IL}=0, V_M=0.6V	C_L=50pF		3.5	7.25	ns
				C_L=15pF		2.2	6.85	ns
Propagation Delay From Input (A or B) to Output (B or A)	Down	t_{PHL}	V_{REF_A}=1.8V, V_{REF_B}=3.3V, V_{EN}=1.8V, R_L=NA, V_{IH}=3.3V, V_{IL}=0, V_M=1.15V	C_L=50pF		3.5	4.9	ns
				C_L=15pF		1.5	4.5	ns
			V_{REF_A}=1.2V, V_{REF_B}=3.3V, V_{EN}=1.2V, R_L=NA, V_{IH}=3.3V, V_{IL}=0, V_M=0.85V	C_L=50pF		0.7	4.7	ns
				C_L=15pF		0.3	4.3	ns
	Up		V_{REF_A}=1.8V, V_{REF_B}=3.3V, V_{EN}=1.8V, R_L=500Ω, V_{IH}=1.8V, V_{IL}=0, V_M=0.9V	C_L=50pF		1.3	6.7	ns
				C_L=15pF		0.7	5.3	ns
			V_{REF_A}=1.2V, V_{REF_B}=1.8V, V_{EN}=1.2V, R_L=500Ω, V_{IH}=1.2V, V_{IL}=0, V_M=0.6V	C_L=50pF		5.5	7.03	ns
				C_L=15pF		2.3	5.4	ns
Output Enable Time From Input (A or B) to Output (B or A)	Down	t_{PLZ}	V_{REF_A}=1.8V, V_{REF_B}=3.3V, V_{EN}=1.8V, R_L=NA, V_{IH}=3.3V, V_{IL}=0, V_M=1.15V	C_L=50pF		13.2	18	ns
				C_L=15pF		9.6	15	ns
	Up		V_{REF_A}=1.8V, V_{REF_B}=3.3V, V_{EN}=1.8V, R_L=500Ω, V_{IH}=1.8V, V_{IL}=0, V_M=0.9V	C_L=50pF		10.8	18	ns
				C_L=15pF		9.2	15	ns
	Down	t_{PZL}	V_{REF_A}=1.8V, V_{REF_B}=3.3V, V_{EN}=1.8V, R_L=NA, V_{IH}=3.3V, V_{IL}=0, V_M=1.15V	C_L=50pF		17	45	ns
				C_L=15pF		11.7	37	ns
	Up		V_{REF_A}=1.8V, V_{REF_B}=3.3V, V_{EN}=1.8V, R_L=500Ω, V_{IH}=1.8V, V_{IL}=0, V_M=0.9V	C_L=50pF		18.2	45	ns
				C_L=15pF		13.8	37	ns
Frequency Response From Input (A or B) to Output (B or A)	Down	f_{MAX}	V_{REF_A}=1.8V, V_{REF_B}=3.3V, V_{EN}=1.8V, R_L=NA, V_{IH}=3.3V, V_{IL}=0, V_M=1.15V	C_L=50pF		50		MHz
				C_L=15pF		100		MHz
			V_{REF_A}=1.2V, V_{REF_B}=3.3V, V_{EN}=1.2V, R_L=NA, V_{IH}=3.3V, V_{IL}=0, V_M=0.85V	C_L=50pF		50		MHz
				C_L=15pF		100		MHz
	Up		V_{REF_A}=1.8V, V_{REF_B}=3.3V, V_{EN}=1.8V, R_L=500Ω, V_{IH}=1.8V, V_{IL}=0, V_M=0.9V	C_L=50pF		50		MHz
				C_L=15pF		100		MHz
			V_{REF_A}=1.2V, V_{REF_B}=1.8V, V_{EN}=1.2V, R_L=500Ω, V_{IH}=1.2V, V_{IL}=0, V_M=0.6V	C_L=50pF		50		MHz
				C_L=15pF		100		MHz

■ TEST CIRCUIT AND WAVEFORMS

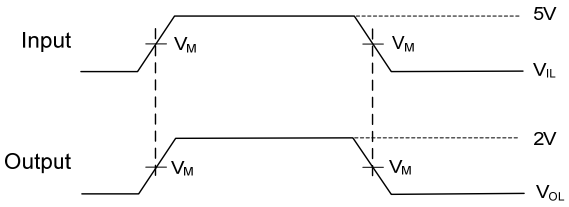


USAGE	SW
Translating Up	S1
Translating Down	S2

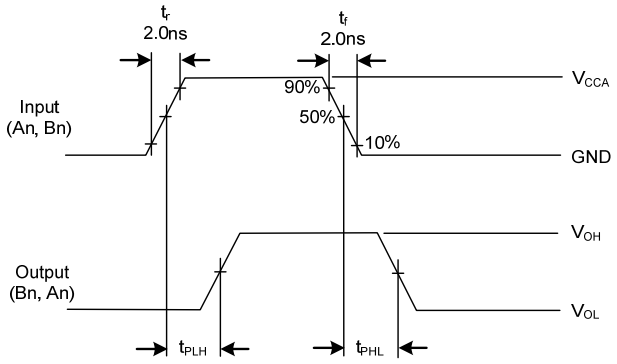
LOAD CIRCUIT



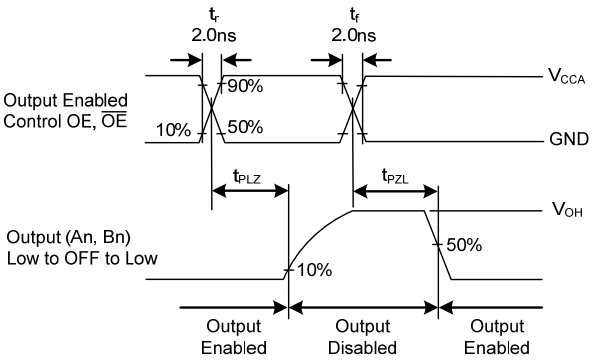
TRANSLATING UP



TRANSLATING DOWN



LOAD CIRCUIT AC WAVEFORM FOR OUTPUTS FOR t_{PLH}, t_{PHL}



LOAD CIRCUIT AC WAVEFORM FOR OUTPUTS FOR t_{PLZ}, t_{PZL}

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: $P_{RR} \leq$ 10MHz, Z_O = 50Ω, $t_r \leq$ 2 ns, $t_f \leq$ 2 ns.

3.The outputs are measured one at a time, with one transition per measurement.

■ DETAILED DESCRIPTION

Overview

The UTC **ULSF0204/D** family may be used in level translation applications for interfacing devices or systems operating at different interface voltages with one another. The UTC **ULSF0204/D** family is ideal for use in applications where an open-drain driver is connected to the data I/Os. The UTC **ULSF0204/D** can achieve 100MHz with appropriate pull-up resistors and layout. The UTC **ULSF0204/D** family can also be used in applications where a push-pull driver is connected to the data I/Os.

■ FEATURE DESCRIPTION

The supply voltage ($V_{PU\#}$) for each channel can be individually setup with a pull-up resistor. For example, CH1 can be used in up-translation mode (1.2V↔3.3V) and CH2 in down-translation mode (2.5V↔1.8V).

When EN is HIGH, the translator switch is on, and the An I/O is connected to the Bn I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by V_{REF}_A. EN must be LOW to ensure the high-impedance state during power-up or power-down.

Table 1. Device Comparison Table

PART NUMBER	EN	An	Bn	DESCRIPTION
ULSF0204	H	Input or output	Input or output	3-state output mode enable (active High; referenced to V_{REF}_A)
	L	Place all data pins in 3 state mode (Hi-Z)	Place all data pins in 3 state mode (Hi-Z)	
ULSF0204D	H	Place all data pins in 3 state mode (Hi-Z)	Place all data pins in 3 state mode (Hi-Z)	3-state output mode enable (active Low; referenced to V_{REF}_A)
	L	Input or output	Input or output	

■ APPLICATION INFORMATION

The UTC **ULSF0204/D** devices are able to perform voltage translation for open-drain or push-pull interface. Table 2 provides some consumer/telecom interfaces as reference in regards to the different channel numbers that are supported by the UTC **ULSF0204/D** family.

Table 2. Voltage Translator for Consumer / Telecom Interface

Part Name	Channel Number	Interface
ULSF0204/D	4	GPIO, MDIO, SM Bus, PM Bus, I^2C, SVIO, UART, SPI

Pull-up Resistor Sizing

The pull-up resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15mA.This ensures a pass voltage of 260mV to 350mV. If the current through the pass transistor is higher than 15mA,the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15mA, to calculate the pull-up resistor value use the following equation:

$$R_{pu} = (V_{PU} - 0.35V) / 0.015A$$

■ APPLICATION INFORMATION (Cont.)

Table 2 summarizes resistor values, reference voltages, and currentsat 15mA,10mA and 3mA. The resistor value shown in the +10% column(or a larger value)should be used to ensure that the pass voltage of the transistor is 350mV or less. The external driver must be able to sink the total current from the resistors on both sides of the UTC **ULSF0204/D** family device at 0.175V, although the 15mA applies only to current flowing through the UTC **ULSF0204/D** family device.

Table 2. Pull-up Resistor Values

V_{DPU}	15mA		10mA		3mA	
	NOMINAL	±10%	NOMINAL	±10%	NOMINAL	±10%
5V	310	341	465	512	1550	1705
3.3V	197	217	295	325	983	1082
2.5V	143	158	215	237	717	788
1.8V	97	106	145	160	483	532
1.5V	77	85	115	127	383	422
1.2V	57	63	85	94	283	312

Family Bandwidth

The maximum frequency of the the UTC **ULSF0204/D** family is dependent on the application. The device can operate at speeds of >100 MHz gave the correct conditions. The maximum frequency is dependent upon the loading of the application. The UTC **ULSF0204/D** family behaves like a standard switch where the bandwidth of the device is dictated by the on resistance and on capacitance of the device.

The 3dB point of the UTC **ULSF0204/D** family is ≈ 600MHz; however, this measurement is an analog type of measurement. For digital applications the signal should not degrade up to the fifth harmonic of the digital signal. The frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is very important in determining the overall shape of the digital signal. In the case of the UTC **ULSF0204/D** family, a digital clock frequency of greater than 100MHz can be achieved.

The UTC **ULSF0204/D** family does not provide any drive capability. Therefore higher frequency applications will require higher drive strength from the host side. No pull-up resistor is needed on the host side(3.3 V)if the UTC **ULSF0204/D** family is being driven by standard CMOS totem pole output driver. Ideally, it is best to minimize the trace length from the UTC **ULSF0204/D** family on the sink side(1.8V) to minimize signal degradation.

All fast edges have an infinite spectrum of frequency components; however, there is an inflection (or knee)in the frequency spectrum of fast edges where frequency components higher than f_{knee} are insignificant in determining the shape of the signal.

To calculate the maximum practical frequency component, or the knee frequency (f_{knee}), use the following equations:

$$f_{knee} = 0.5 / RT \ (10\text{-}80\%)$$
$$f_{knee} = 0.4 / RT \ (20\text{-}80\%)$$

For signals with rise time characteristics based on 10% to 90% thresholds, f_{knee} is equal to 0.5 divided by the rise time of the signal. For signals with rise time characteristics based on 20% to 80% thresholds, which his very common in many of today's device specifications, f_{knee} is equal to 0.4 divided by the rise time of the signal.

- Keep trace length to a minimum by placing the UTC **ULSF0204/D** family close to the I^2Coutputofthe processor.
- The trace length should be less than half the time off light to reduce ringing and line reflections or non-monotonic behavior in the switching region.
- To reduce overshoots a pull-up resistor can be added on the 1.8V side; be aware that as lower fall time is to be expected.

Power Supply Recommendations

There are no power sequence requirements for the UTC **ULSF0204/D** family. For enable and reference voltage guidelines, please refer to the Enable, Disable, and Reference Voltage Guidelines.

■ TYPICAL APPLICATION CIRCUIT

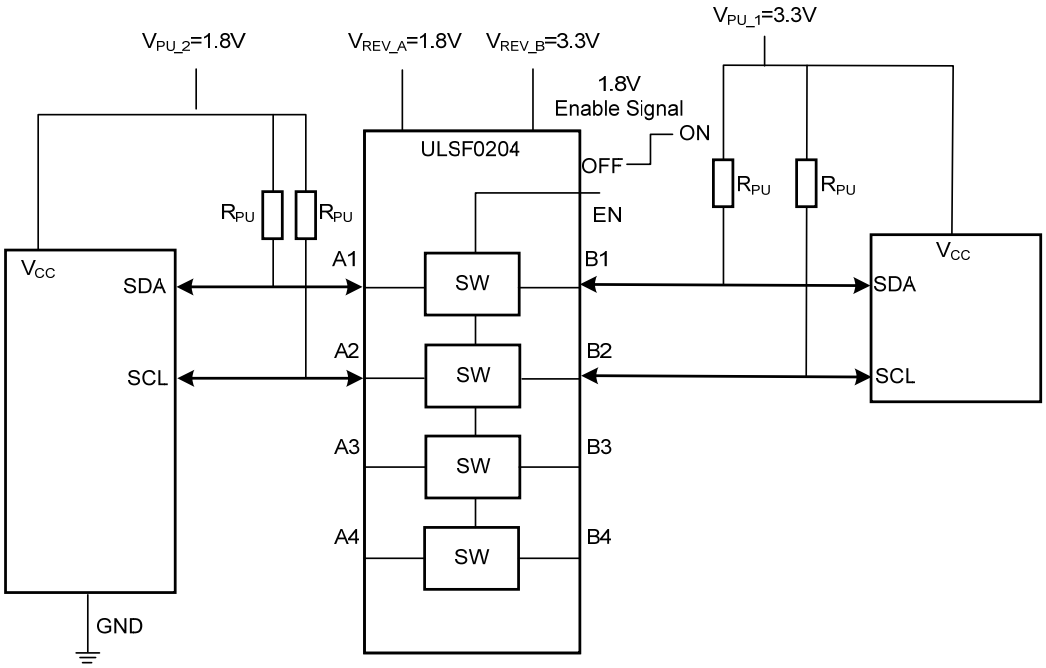


Figure 1. Bidirectional Translation to Multiple Voltage Levels

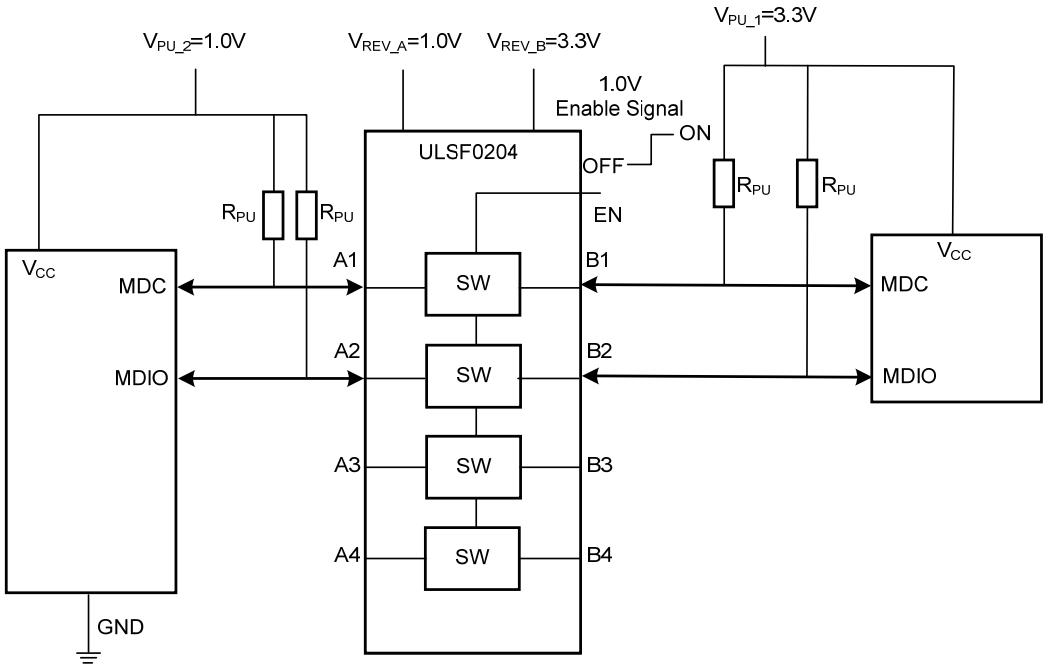


Figure 2. Typical Application Circuit (MDIO/Bidirectional Interface)

■ TYPICAL APPLICATION CIRCUIT (Cont.)

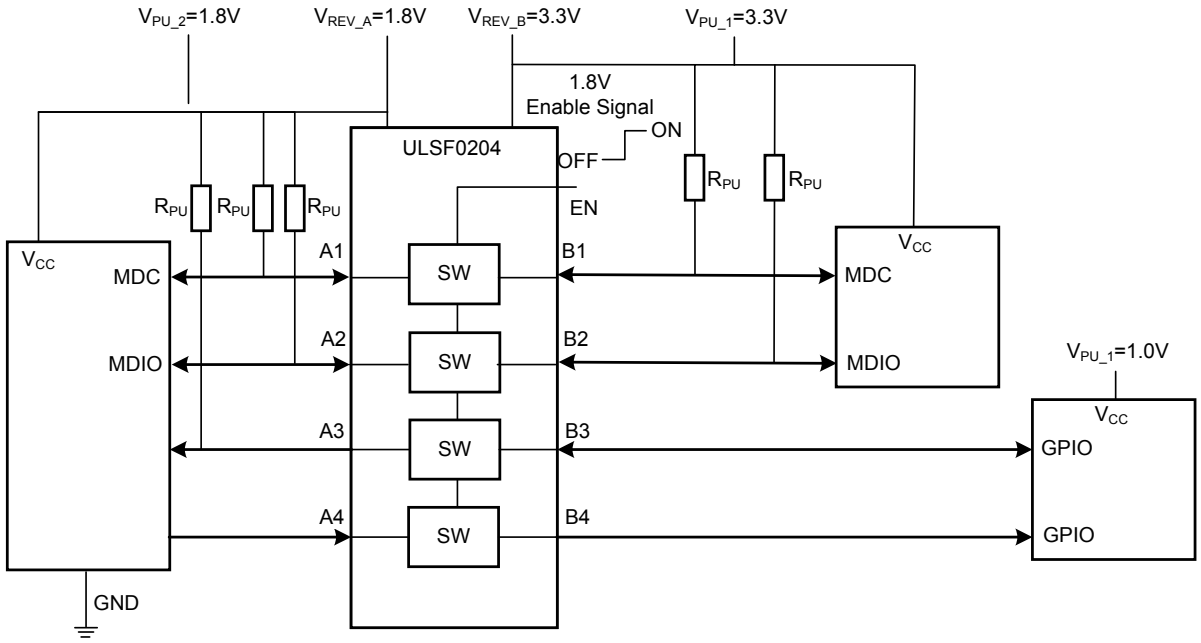


Figure 3. Multiple Voltage Translation in Single Device, Application