

11N40K-MT

Power MOSFET

11.4A, 400V N-CHANNEL POWER MOSFET

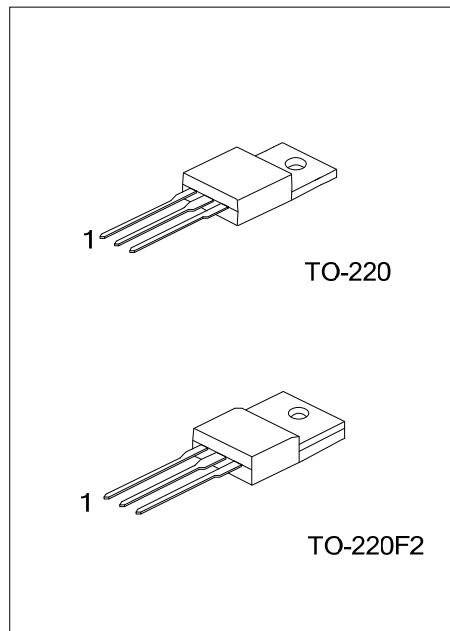
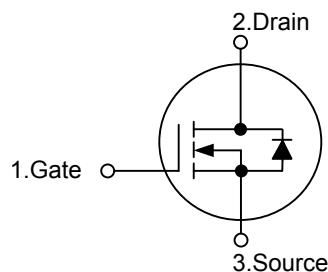
■ DESCRIPTION

The **11N40K-MT** uses UTC's advanced proprietary, planar stripe, DMOS technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with low gate voltages. This device is suitable for use as a load switch or in PWM applications.

■ FEATURES

- * $R_{DS(ON)} < 0.52\Omega$ @ $V_{GS} = 10$ V, $I_D = 5.7$ A
- * Fast Switching Capability
- * Avalanche Energy Specified
- * Improved dv/dt Capability, High Ruggedness

■ SYMBOL



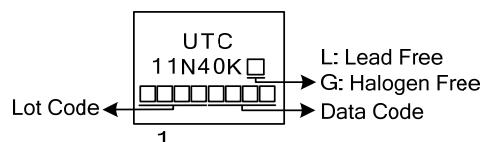
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
11N40KL-TA3-T	11N40KG-TA3-T	TO-220	G	D	S	Tube
11N40KL-TF2-T	11N40KG-TF2-T	TO-220F2	G	D	S	Tube

Note: Pin Assignment: G: GND D: Drain S: Source

11N40KL-TA3-T 	(1) T: Tube (2) TA3: TO-220, TF2: TO-220F2 (3) L: Lead Free, G: Halogen Free and Lead Free
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■ MARKING



■ ABSOLUTE MAXIMUM RATING (T_C =25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V _{DSS}	400	V
Gate-Source Voltage	V _{GSS}	±30	V
Continuous Drain Current (T _C = 25°C)	I _D	11.4	A
Pulsed Drain Current (Note 2)	I _{DM}	46	A
Avalanche Current (Note 2)	I _{AR}	11.4	A
Avalanche Energy	Single Pulsed(Note 3)	E _{AS}	mJ
	Repetitive(Note 2)	E _{AR}	
Peak Diode Recovery dv/dt (Note 4)	dv/dt	4.5	V/ns
Power Dissipation	TO-220	147	W
	TO-220F2	35	W
Derate above 25°C	TO-220	1.176	W/°C
	TO-220F2	0.28	W/°C
Junction Temperature	T _J	150	°C
Storage Temperature	T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. L=7mH, I_{AS}=11.4A, V_{DD}=50V, R_G=25Ω, Satarting T_J=25°C

4. I_{SD} ≤ 11.4A, di/dt ≤ 200A/μs, V_{DD} ≤BV_{DSS}, Satarting T_J=25°C

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ _{JA}	62.5	°C/W
Junction to Case	TO-220	0.85	°C/W
	TO-220F2	3.86	°C/W

■ ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}} = 0 \text{ V}, I_D = 250 \mu\text{A}$	400			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 400 \text{ V}, V_{\text{GS}} = 0 \text{ V}$		1		μA
		$V_{\text{DS}} = 320 \text{ V}, T_C = 125^\circ\text{C}$		10		
Gate-Body Leakage Current	I_{GSS}	$V_{\text{DS}} = 0 \text{ V}, V_{\text{GS}} = \pm 30 \text{ V}$			± 100	nA
Breakdown Voltage Temperature Coefficient	$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	$I_D = 250 \mu\text{A}$, Referenced to 25°C	0.42			mV/ $^\circ\text{C}$
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{\text{GS(TH)}}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250 \mu\text{A}$	2.0		4.0	V
Static Drain-Source On-Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}} = 10 \text{ V}, I_D = 5.7 \text{ A}$		0.37	0.52	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{\text{DS}} = 25 \text{ V}, V_{\text{GS}} = 0 \text{ V}, f = 1 \text{ MHz}$		670	970	pF
Output Capacitance	C_{OSS}			135	195	
Reverse Transfer Capacitance	C_{RSS}			8.9	15	
SWITCHING PARAMETERS						
Turn-ON Delay Time	$t_{\text{D(ON)}}$	$V_{\text{DD}} = 30 \text{ V}, I_D = 0.5 \text{ A}, R_{\text{GEN}} = 25 \Omega$ (Note 1, 2)		60		ns
Turn-ON Rise Time	t_R			88		
Turn-OFF Delay Time	$t_{\text{D(OFF)}}$			150		
Turn-OFF Fall-Time	t_F			85		
Total Gate Charge	Q_G	$V_{\text{DS}} = 50 \text{ V}, V_{\text{GS}} = 10 \text{ V}, I_D = 1.3 \text{ A}$ (Note 1, 2)		27	35	nC
Gate Source Charge	Q_{GS}			8.9		
Gate Drain Charge	Q_{GD}			6.6		
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V_{SD}	$I_S = 11.4 \text{ A}, V_{\text{GS}} = 0 \text{ V}$			1.5	V
Maximum Body-Diode Continuous Current	I_S				11.4	A
Maximum Body-Diode Pulsed Current	I_{SM}				46	A

Notes: 1. Pulse Test: Pulse Width $\leq 300 \text{ s}$, Duty Cycle $\leq 2\%$

2. Independent of operating temperature

■ TEST CIRCUIT

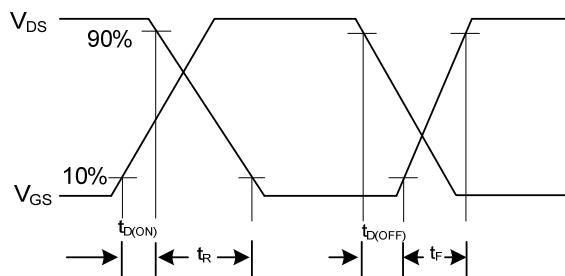
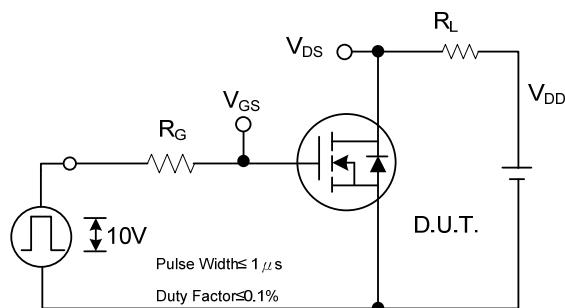


Fig. 2A Switching Test Circuit

Fig. 2B Switching Waveforms

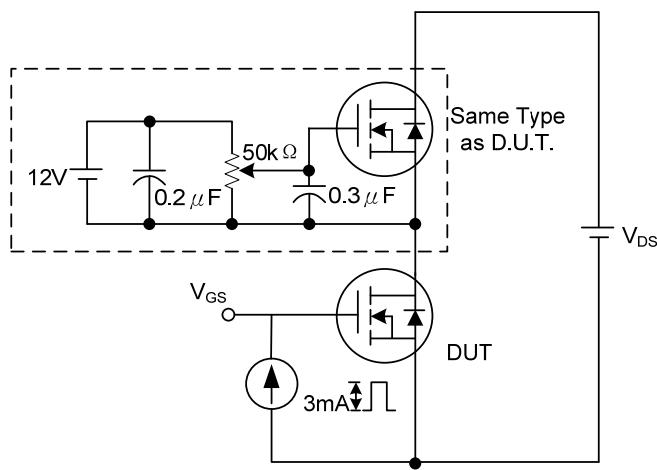


Fig. 3A Gate Charge Test Circuit

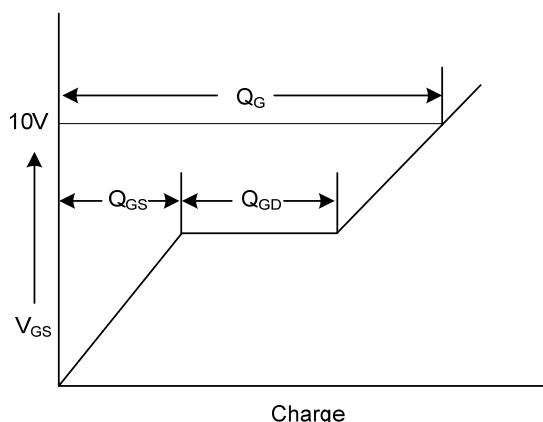


Fig. 3B Gate Charge Waveform

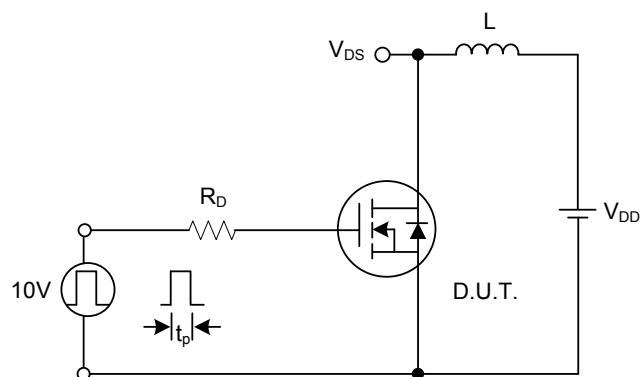


Fig. 4A Unclamped Inductive Switching Test Circuit

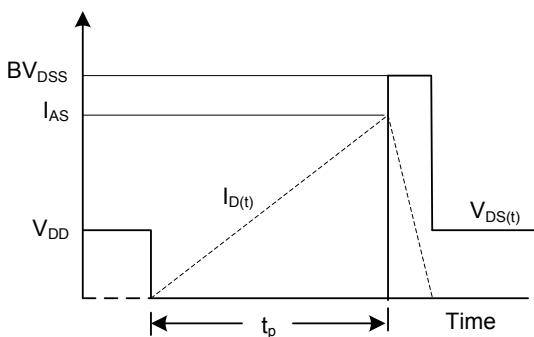
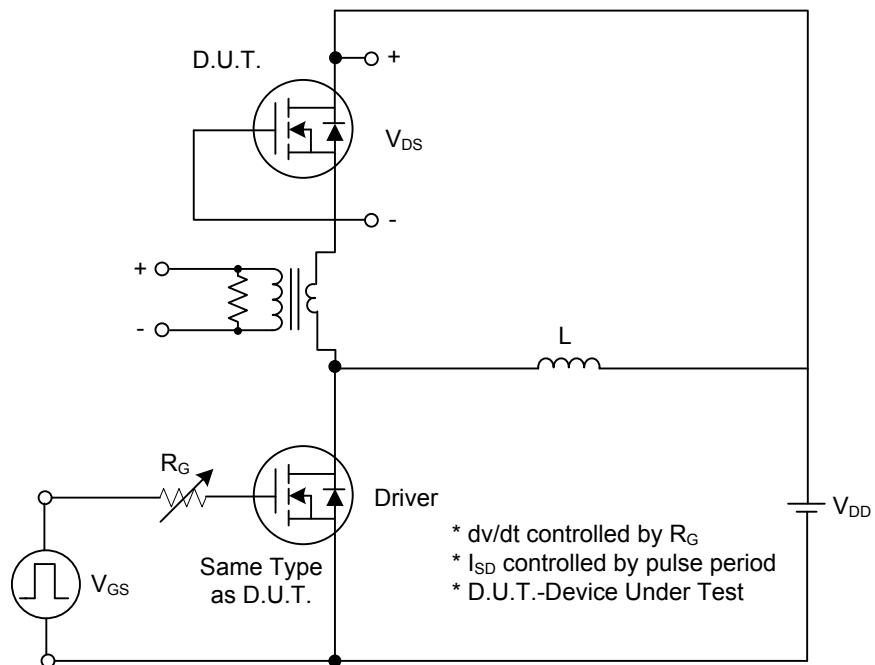
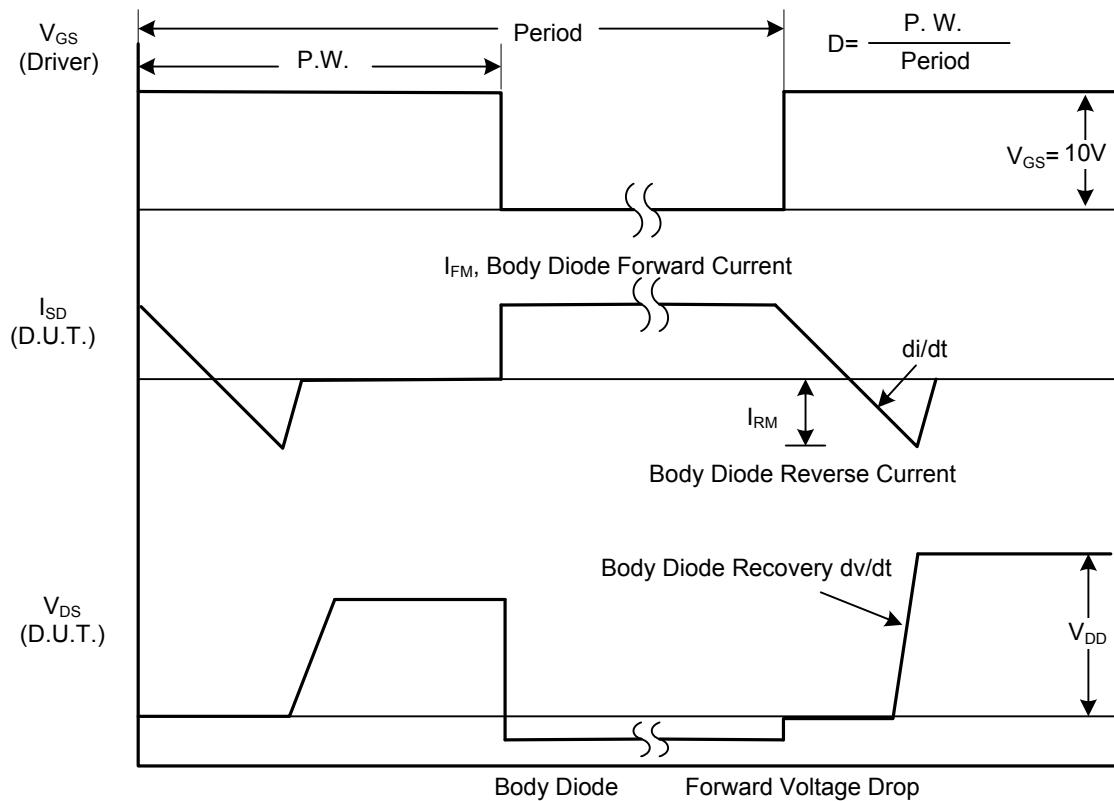
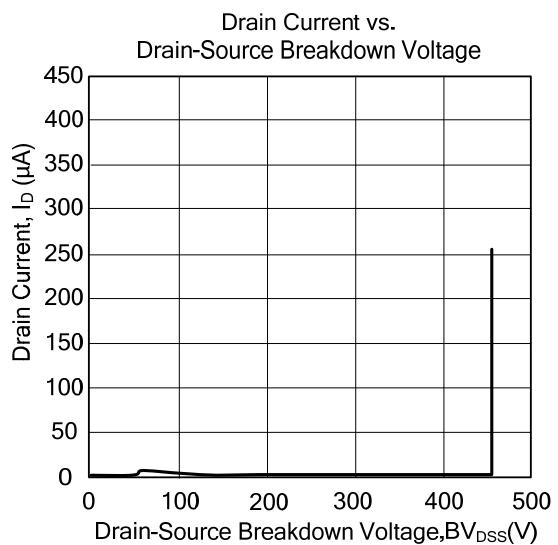
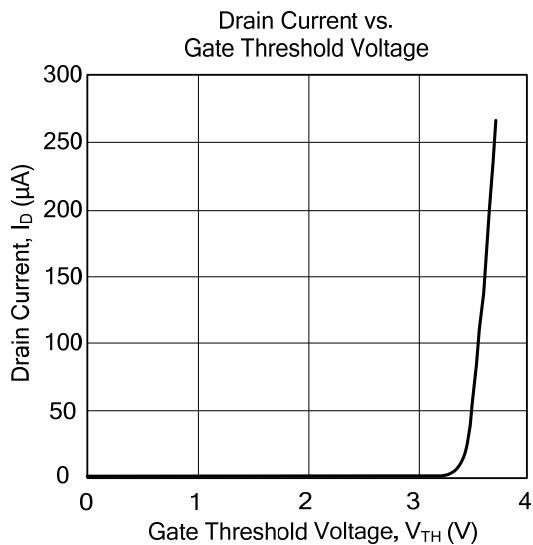
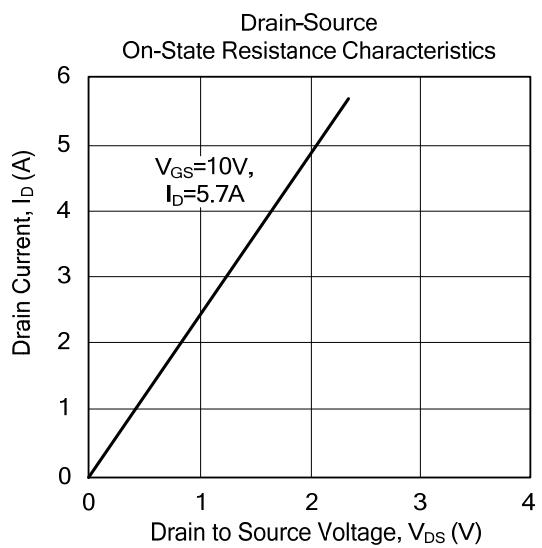
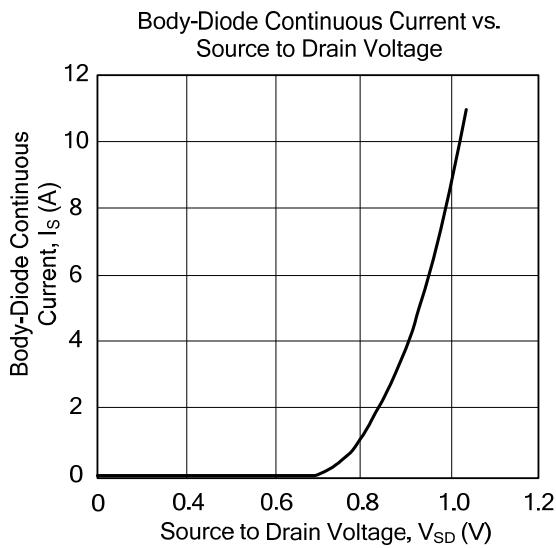


Fig. 4B Unclamped Inductive Switching Waveforms

■ TEST CIRCUIT(Cont.)

Fig. 1A Peak Diode Recovery dv/dt Test Circuit

■ TYPICAL CHARACTERISTICS



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