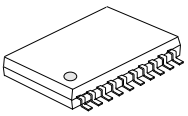
U74CB3Q3245 **Advance** ***CMOS IC***

8-BIT FET BUS SWITCH 2.5V-/3.3V LOW-VOLTAGE HIGH BANDWIDTH BUS SWITCH



TSSOP-20

■ DESCRIPTION

The **U74CB3Q3245** is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (R_{ON}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, The UTC **U74CB3Q3245** provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The UTC **U74CB3Q3245** is organized as an 8-bit bus switch with a single output-enable($\overline{OE}$) input. When $\overline{OE}$ is low, the bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the bus switch is OFF and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

■ FEATURES

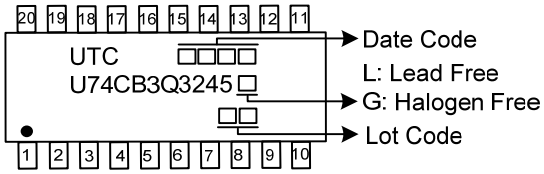
* High-Bandwidth Data Path(up to 500MHz)
* 5V Tolerant I/Os With Device Powered Up or Powered Down
* Low and Flat ON-State Resistance (R_{ON}) Characteristics Over Operating Range (R_{ON}=4Ω Typ.)
* Rail-to-Rail Switching on Data I/O Ports
  - 0 to 5V Switching With 3.3V V_{CC}
  - 0 to 3.3V Switching With 2.5V V_{CC}
* Bidirectional Data Flow With Near-Zero Propagation Delay
* Low Input / Output Capacitance Minimizes Loading and Signal Distortion($C_{io(OFF)}$=3.5pF Typ.)
* Fast Switching Frequency (f_{OE}=20MHz Max.)
* Data and Control Inputs Provide Undershoot Clamp Diodes
* Low Power Consumption (I_{CC}=1mA Typical)
* V_{CC} Operating Range From 2.3V to 3.6V
* Data I/Os Support 0 to 5V Signaling Levels (0.8V,1.2V,1.5V,1.8V,2.5V,3.3V,5V)
* Control Inputs Can Be Driven by TTL or 5V/3.3V CMOS Outputs
* I_{OFF} Supports Partial-Power-Down Mode Operation
* Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

■ ORDERING INFORMATION

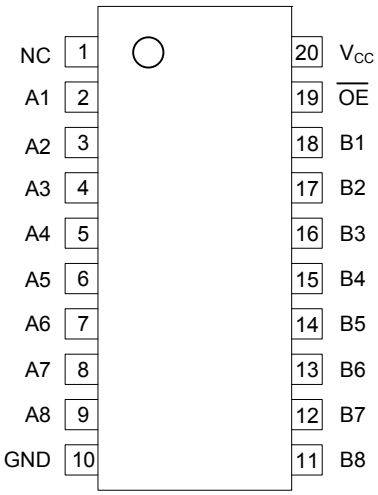
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74CB3Q3245L-P20-R	U74CB3Q3245G-P20-R	TSSOP-20	Tape Reel

U74CB3Q3245G-P20-R (1)Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) P20: TSSOP-20 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



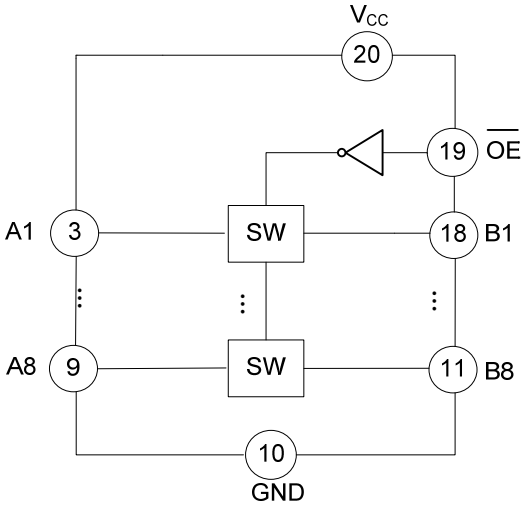
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	NC		No connection
2-9	An	I/O	Input/output An
10	GND		Ground
11 ~18	Bn	I/O	Input/output Bn
19	$\overline{OE}$	I	Pull OE low, An =Bn
20	V_{CC}		Supply Voltage 1.65V ≤ V_{CCB} ≤ 5.5V

■ LOGIC DIAGRAM (positive logic)



■ FUNCTION TABLE

INPUT	INPUT/OUTPUT	FUNICTION
$\overline{OE}$	A	
L	B	A Port = B Port
H	Z	Disconnect

■ ABSOLUTE MAXIMUM RATING (unless otherwise specified) (Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 4.6	V
Input Voltage	V_{IN}		-0.5 ~ 7	V
Switch I/O voltage range	$V_{I/O}$		-0.5 ~ 7	V
Input Clamp Current	I_{IK}	V_{IN}<0V	-50	mA
I/O Port Clamp Current	$I_{I/OK}$	$V_{I/O}$<0V	-50	mA
On state switch current	I_{OK}	V_{OUT}<0V	±64	mA
Continuous current through V_{CC} or GND (Note 2)			±100	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The value of V_{CC} are provided in the recommended operating conditions table.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.3		3.6	V
High-Level Input Voltage	V_{IH}	V_{CC}=2.3V~2.7V	1.7		5.5	V
		V_{CC}=2.7V~3.6V	2		5.5	V
Low-Level Input Voltage	V_{IL}	V_{CC}=2.3V~2.7V	0		0.7	V
		V_{CC}=2.7V~3.6V	0		0.8	V
Input / Output Voltage	$V_{I/O}$		0		5.5	V
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS

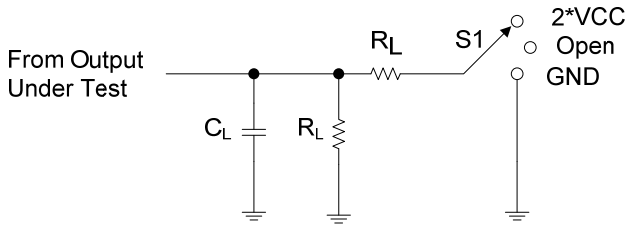
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
Digital Input Diode Voltage	V_{IK}	V_{CC}=3.6V, I_I= -18mA				-1.8	V
Input Leakage Current	I_{IN}	V_{CC}=3.6V,V_{IN} =0V~5.5V				±1	μA
Power OFF Leakage Current	I_{OFF}	V_O=0~5.5V, V_{CC}=0V, V_I=0V				1	μA
Output OFF-State Current	I_{OZ}	V_{CC}=3.6V,V_O=0V~5.5V, VI=0, V_{IN}=V_{CC} or GND, Switch Off				±1	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND, $I_{I/O}$=0A V_{CC}=3.6V, Switch ON or OFF			1	2	mA
Additional Quiescent Supply Current	ΔI_{CC}	V_{CC}=3.6V, one input at 3V, other inputs at V_{CC} or GND				2	mA
Input Capacitance	C_{IN}	V_{CC}=3.3V, V_{IN}=5.5V, 3.3V, 0V			2.5	3.5	pF
I/O Capacitance (OFF)	$C_{IO(OFF)}$	V_{CCA}=3.3V, V_{IN}=5.5V, 3.3V, 0V V_{IN}=V_{CC} or GND, Switch OFF			3.5	5	pF
I/O Capacitance (ON)	$C_{IO(ON)}$	V_{CCA}=3.3V, V_{IN}=5.5V, 3.3V, 0V V_{IN}=V_{CC} or GND, Switch ON			9	11	pF
Resistor Between Two Ports	R_{ON}	V_{CC}=2.3V	V_I=0, I_O=30mA		4	8	Ω
			V_I=1.7, I_O=-15mA		4.5	9	Ω
		V_{CC}=3V	V_I=0, I_O=30mA		4	6	Ω
			V_I=2.4, I_O=-15mA		4	8	Ω

Notes: 1. V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
2. All typical values are at V_{CC}=3.3V (unless otherwise noted), T_A=25°C.

■ SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
From input ($\overline{OE}$) to output (A or B)	$F_{\overline{OE}}$	V_{CC}=2.5V			10	MHz
		V_{CC}=3.3V			20	MHz
From input (A or B) to output (B or A)	t_{pd} (t_{PLH}/t_{PHL})	V_{CC}=2.5V			0.12	ns
		V_{CC}=3.3V			0.2	ns
From input ($\overline{OE}$) to output (A or B)	t_{en} (t_{PZL}/t_{PZH})	V_{CC}=2.5V	1.5		7.5	ns
		V_{CC}=3.3V	1.5		6.5	ns
From input ($\overline{OE}$) to output (A or B)	t_{dis} (t_{PLZ}/t_{PHZ})	V_{CC}=2.5V	1		6.5	ns
		V_{CC}=3.3V	1		6.5	ns

■ TEST CIRCUIT AND WAVEFORMS

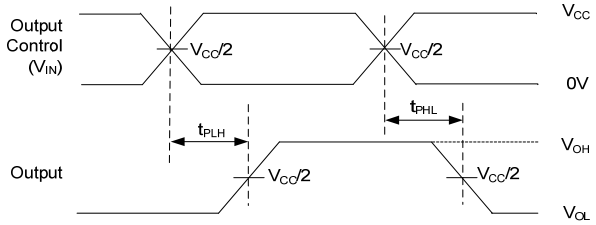


TEST	S1
t_{PLZ}/t_{PZL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

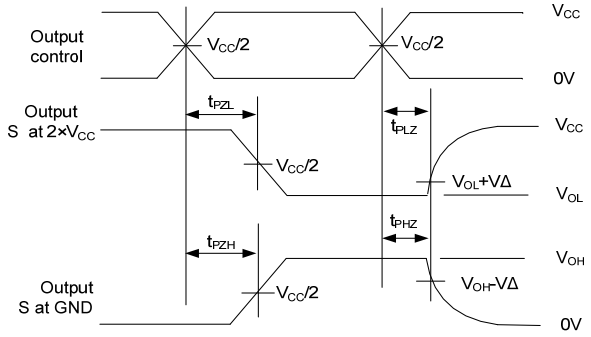
LOAD CIRCUIT

Note: C_L includes probe and jig capacitance.

TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
t_{PD}	2.5V±0.2V	Open	500Ω	V_{CC} or GND	30pF	-
	3.3V±0.3V	Open	500Ω	V_{CC} or GND	50pF	-
t_{PLZ} / t_{PZL}	2.5V±0.2V	2×V_{CC}	500Ω	GND	30pF	0.15V
	3.3V±0.3V	2×V_{CC}	500Ω	GND	50pF	0.3V
t_{PHZ} / t_{PZH}	2.5V±0.2V	GND	500Ω	V_{CC}	30pF	0.15V
	3.3V±0.3V	GND	500Ω	V_{CC}	50pF	0.3V



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
2. The outputs are measured one at a time, with one transition per measurement.
3. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
4. t_{PZL} and t_{PZH} are the same as t_{en}.
5. t_{PLH} and t_{PHL} are the same as t_{PD}(s). The tpd propagation delay is the calculated RC time constant of the typical On-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
6. All parameters and waveforms are not applicable to all devices.