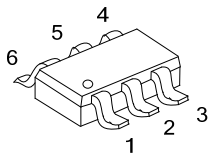
SINGLE D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT



SOT-363

■ DESCRIPTION

The **U74LVC1G374** device is single D-type latch is designed for 1.65V to 5.5V V_{CC} operation.

The **U74LVC1G374** features a 3-state output designed specifically for driving highly capacitive or preventing damaging current backflow relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q output is set to the logic level set up at the data (D) input.

A buffered output-enable ($\overline{OE}$) input can be used to place the output in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the output neither loads nor drives the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pull-up components.

$\overline{OE}$ does not affect the internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

■ FEATURES

* Wide supply voltage range from 1.65V to 5.5V
* Inputs accept voltages up to 5.5V
* I_{OFF} supports partial-power-down mode
* Low static power consumption; I_{CC}=10μA (Max.)

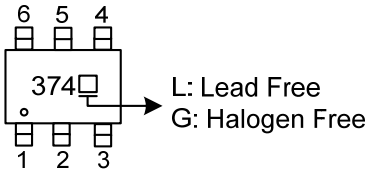
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC1G374L-AL6-R	U74LVC1G374G-AL6-R	SOT-363	Tape Reel

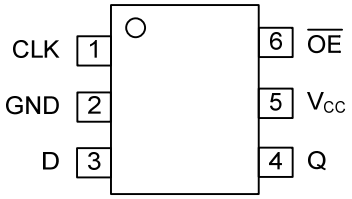
U74LVC1G374G-AL6-R
- (1)Packing Type
- (2)Package Type
- (3)Green Package

(1) R: Tape Reel
(2) AL6: SOT-363
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION



■ PIN DESCRIPTION

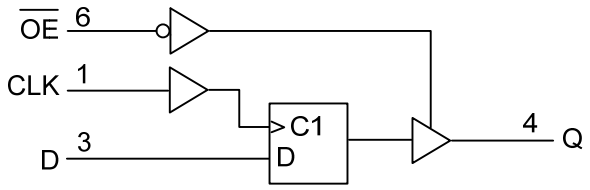
PIN NO.	PIN NAME	I/O	DESCRIPTION
1	CLK	I	Clock input
2	GND	-	Ground
3	D	I	Data input
4	Q	O	Output
5	V_{CC}	-	Power
6	$\overline{OE}$	I	Active low output enable; Hi-Z output when high

■ FUNCTION TABLE

INPUT($\overline{OE}$)	INPUT(CLK)	INPUT(D)	OUTPUT(Q)
L	↑	L	L
L	↑	H	H
L	H or L	X	Q_0
H	X	X	Hi-Z

Note: H: HIGH voltage level, L: LOW voltage level, Q_0: No Change, Hi-Z: High Impedance.

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +6.5	V
Input Voltage	V_{IN}		-0.5 ~ +6.5	V
Output Voltage	V_{OUT}	Output in the high or low state	-0.5 ~ V_{CC} +0.5	V
		Output in the power-off state	-0.5 ~ +6.5	V
Continuous V_{CC} or GND Current	I_{CC}		±100	mA
Continuous Output Current	I_{OUT}		±50	mA
Input Clamp Current	I_{IK}	V_{IN}<0V	-50	mA
Output Clamp Current	I_{OK}	V_{OUT}<0V	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	Δt/Δv	V_{CC}=1.8V±0.15V, 2.5V±0.2V			20	ns/V
		V_{CC}=3.3V±0.3V			10	ns/V
		V_{CC}=5V±0.5V			5	ns/V
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	V_{CC}=1.8±0.15V	0.65×V_{CC}			V
		V_{CC}=2.5±0.2V	1.7			V
		V_{CC}=3.3±0.3V	2			V
		V_{CC}=5±0.5V	0.7×V_{CC}			V
Low-level Input Voltage	V_{IL}	V_{CC}=1.8±0.15V			0.35×V_{CC}	V
		V_{CC}=2.5±0.2V			0.7	V
		V_{CC}=3.3±0.3V			0.8	V
		V_{CC}=5±0.5V			0.3×V_{CC}	V
High-Level Output Voltage	V_{OH}	V_{CC}=1.65 ~ 5.5V, I_{OH}=-100μA	V_{CC}-0.1			V
		V_{CC}=1.65V, I_{OH}=-4mA	1.2			V
		V_{CC}=2.3V, I_{OH}=-8mA	1.9			V
		V_{CC}=3.0V, I_{OH}=-16mA	2.4			V
		V_{CC}=3.0V, I_{OH}=-24mA	2.3			V
		V_{CC}=4.5V, I_{OH}=-32mA	3.8			V
Low-Level Output Voltage	V_{OL}	V_{CC}=1.65 ~ 5.5V, I_{OL}=100μA			0.1	V
		V_{CC}=1.65V, I_{OL}=4mA			0.45	V
		V_{CC}=2.3V, I_{OL}=8mA			0.3	V
		V_{CC}=3.0V, I_{OH}=16mA			0.4	V
		V_{CC}=3.0V, I_{OH}=24mA			0.55	V
		V_{CC}=4.5V, I_{OL}=32mA			0.55	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=1.65V ~ 5.5V V_{IN}=V_{CC} or GND			±1	μA
Power Off Leakage Current	I_{OFF}	V_{CC}=0V, V_{IN} or V_{OUT}=5.5V			±10	μA
OFF-state output current	I_{OZ}	V_{OUT}=0~5.5V			±5	μA

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Supply Current	I_{CC}	V_{CC}=1.65 ~ 5.5V, V_{IN}=5.5V or GND, I_{OUT}=0			10	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	V_{CC}=3 ~ 5.5V, One input at V_{CC}-0.6V, other inputs at V_{CC} or GND			500	μA
Input Capacitance	C_{IN}	V_{CC}=3.3V, V_{IN}=V_{CC} or GND		3		pF
Output Capacitance	C_{OUT}	V_{CC}=3.3V, V_{IN}=V_{CC} or GND		6		pF

■ TIMING REQUIREMENTS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Frequency	f_{CLOCK}	V_{CC}=1.8±0.15V			80	MHz
		V_{CC}=2.5±0.2V			125	MHz
		V_{CC}=3.3±0.3V			150	MHz
		V_{CC}=5±0.5V			175	MHz
Pulse Duration, CLK High or Low	t_w	V_{CC}=1.8±0.15V	3.3			ns
		V_{CC}=2.5±0.2V	3.0			ns
		V_{CC}=3.3±0.3V	2.8			ns
		V_{CC}=5±0.5V	2.5			ns
Setup Time, Data Before CLK↑	t_{su}	V_{CC}=1.8±0.15V	3.5			ns
		V_{CC}=2.5±0.2V	2.5			ns
		V_{CC}=3.3±0.3V	2.0			ns
		V_{CC}=5±0.5V	1.5			ns
Hold Time, Data After CLK↑	t_h	V_{CC}=1.8±0.15V	3.4			ns
		V_{CC}=2.5±0.2V	1.6			ns
		V_{CC}=3.3±0.3V	1.5			ns
		V_{CC}=5±0.5V	1.5			ns

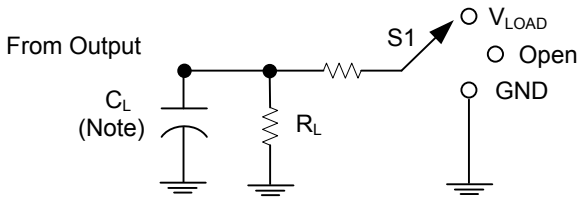
■ SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Maximum clock pulse frequency	f_{MAX}	V_{CC}=1.8V±0.15V	C_L=30pF or 50pF	80			MHz
		V_{CC}=2.5V±0.2V		125			MHz
		V_{CC}=3.3V±0.3V		150			MHz
		V_{CC}=5.0V±0.5V		175			MHz
Propagation delay from input (CLK) to output (Q)	t_{PD}	V_{CC}=1.8V±0.15V	C_L=30pF or 50pF	2.7		18.3	ns
		V_{CC}=2.5V±0.2V		1.8		12.2	ns
		V_{CC}=3.3V±0.3V		1.6		9.5	ns
		V_{CC}=5.0V±0.5V		1.0		7.5	ns
Propagation delay from input ($\overline{OE}$) to output (Q)	t_{en}	V_{CC}=1.8V±0.15V	C_L=30pF or 50pF	2.0		14	ns
		V_{CC}=2.5V±0.2V		1.5		12	ns
		V_{CC}=3.3V±0.3V		0.9		9.0	ns
		V_{CC}=5.0V±0.5V		0.7		6.5	ns
Propagation delay from input ($\overline{OE}$) to output (Q)	t_{dis}	V_{CC}=1.8V±0.15V	C_L=30pF or 50pF	2.0		13	ns
		V_{CC}=2.5V±0.2V		1.1		8.3	ns
		V_{CC}=3.3V±0.3V		1.4		6.5	ns
		V_{CC}=5.0V±0.5V		0.8		5.1	ns

■ OPERATING CHARACTERISTICS (f=10MHz, T_A=25°C , unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Output enabled	C_{PD}	V_{CC}=1.8V		24		pF
			V_{CC}=2.5V		24		pF
			V_{CC}=3.3V		25		pF
			V_{CC}=5V		27		pF
	Output disabled		V_{CC}=1.8V		8		pF
			V_{CC}=2.5V		8		pF
			V_{CC}=3.3V		9		pF
			V_{CC}=5V		11		pF

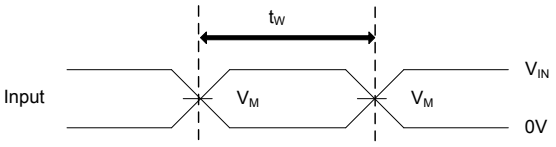
■ TEST CIRCUIT AND WAVEFORMS



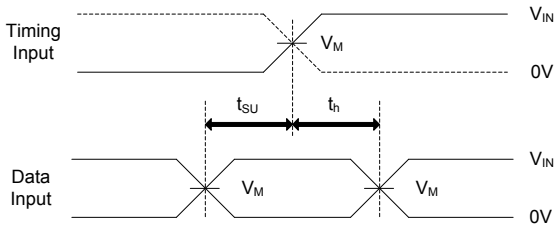
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

Note: C_L includes probe and jig capacitance.

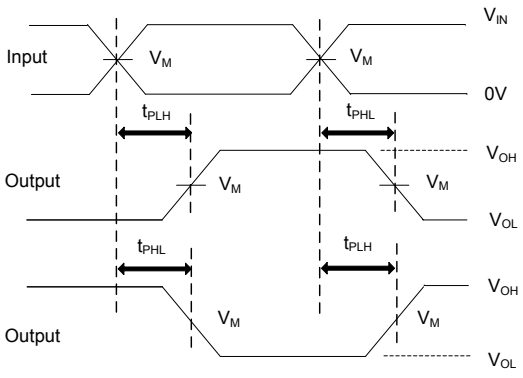
V_{CC}	V_{IN}	t_R / t_F	V_M	V_{LOAD}	C_L	R_L	V_Δ
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	1KΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	$2\times V_{CC}$	30pF	500Ω	0.15V
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	$2\times V_{CC}$	50pF	500Ω	0.3V



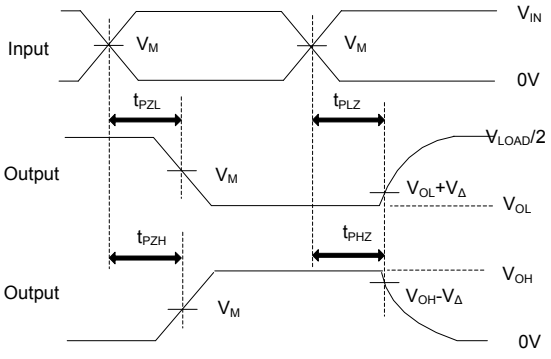
PULSE WIDTH



SETUP TIME AND HOLD TIME



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω.
3. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
4. t_{PZL} and t_{PZH} are the same as t_{en}.
5. t_{PLH} and t_{PHL} are the same as t_{PD}.