

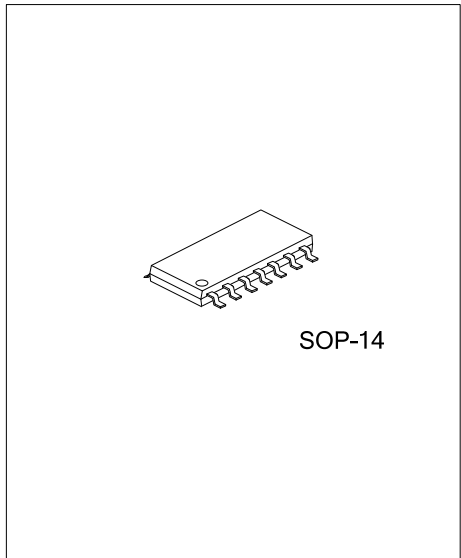


U74AHCT132

Preliminary

CMOS IC

QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT-TRIGGER INPUTS



SOP-14

DESCRIPTION

The **U74AHCT132** is a device is a quadruple positive NAND gate designed for 2V to 5.5V V_{CC} operation. This device performs the Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A + B}$ in positive logic.

FEATURES

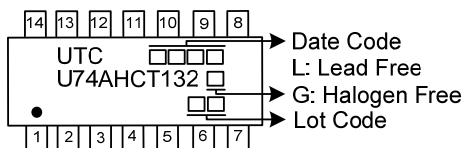
- * Operate from 4.5V to 5.5V
- * Operation form very slow input transitions
- * Temperature-Compensated threshold levels
- * Balanced propagation delays
- * Inputs accepts voltages higher than V_{CC}

ORDERING INFORMATION

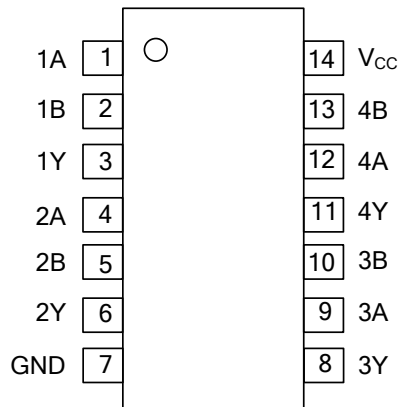
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHCT132L-S14-R	U74AHCT132G-S14-R	SOP-14	Tape Reel

<p>U74AHCT132G-S14-R</p>	<p>(1) R: Tape Reel (2) S14: SOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ PIN CONFIGURATION

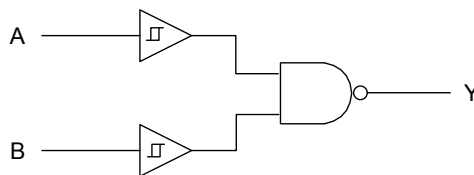


■ FUNCTION TABLE

INPUT(A)	INPUT(B)	OUTPUT(Y)
H	H	L
L	X	H
X	L	H

H = High voltage level ; L = Low voltage level ; X = Don't care

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V _{CC}		-0.5 ~ 7	V
Input Voltage (Note 2)	V _{IN}	V _{OUT} <0 or V _{OUT} >V _{CC}	-0.5 ~ 7	V
Output Voltage	V _{OUT}		-0.5 ~ V _{CC} +0.5	V
Continuous current through V _{CC} or GND	I _{CC}		±50	mA
Input Clamp Current	I _{IK}	V _{IN} <0	-20	mA
Output Clamp Current	I _{OK}	V _{OUT} < 0 or V _{OUT} > V _{CC}	±20	mA
Continuous Output Current	I _{OUT}	V _{OUT} < 0 to V _{CC}	±25	mA
Storage Temperature	T _{STG}		-65 ~ + 150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}		4.5		5.5	V
Input Voltage	V _{IN}		0		5.5	V
Output Voltage	V _{OUT}		0		V _{CC}	V
Operating Temperature	T _A		-40		+125	°C

Note: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive-Going Input Threshold Voltage	V _{T+}	V _{CC} =4.5V	0.9		1.9	V
		V _{CC} =5.5V	1.0		2.1	V
Negative-Going Input Threshold Voltage	V _{T-}	V _{CC} =4.5V	0.5		1.5	V
		V _{CC} =5.5V	0.6		1.7	V
Hysteresis (V _{T+} -V _{T-})	ΔV _T	V _{CC} =4.5V	0.3		1.4	V
		V _{CC} =5.5V	0.3		1.5	V
High-Level Output Voltage	V _{OH}	V _{CC} =4.5V, I _{OH} =-50mA	4.4	4.5		V
		V _{CC} =4.5V, I _{OH} =-8mA	3.94			V
Low-Level Output Voltage	V _{OL}	V _{CC} =4.5V, I _{OH} =-50mA			0.1	V
		V _{CC} =4.5V, I _{OH} =-8mA			0.36	V
Input Leakage Current	I _{I(LEAK)}	V _{CC} =0~5.5V, V _{IN} =5.5V or GND			±0.1	μA
Quiescent Supply Current	I _Q	V _{CC} =5.5V, V _{IN} =V _{CC} or GND, I _{OUT} =0A			2	μA
Additional Quiescent Supply Current Per Input Pin	ΔI _Q	V _{CC} =5.5V, One Input at 3.4V, Other Inputs at V _{CC} or GND			1.35	mA
Input Capacitance	C _{IN}	V _{CC} =5.0V, V _{IN} =V _{CC} or GND		2	10	pF

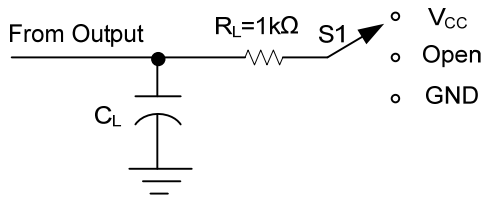
■ SWITCHING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Propagation Delay From Input (A or B) to Output (Y)	t _{PLH}	V _{CC} =5V±0.5V	C _L =15pF		6.4	8.0	ns
			C _L =50pF		9.5	12	ns
	t _{PHL}		C _L =15pF		3.0	6.0	ns
			C _L =50pF		3.2	7.0	ns

■ OPERATING CHARACTERISTICS (T_A=25°C, unless otherwise specified)

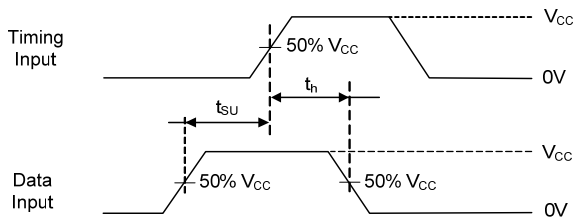
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance Per Flip-Flop	C _{PD}	V _{CC} =5V, f=1MHz, No load.		15		pF

■ TEST CIRCUIT AND WAVEFORMS

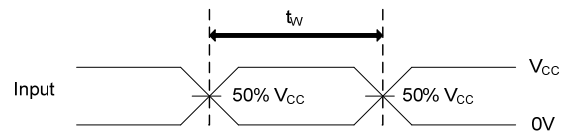


TEST CIRCUIT

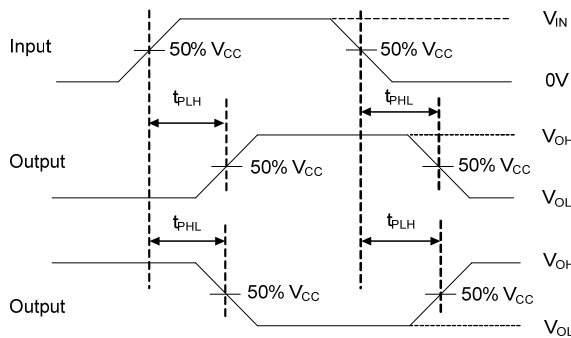
TEST	S1
t_{PLZ}/t_{PZL}	V_{CC}
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



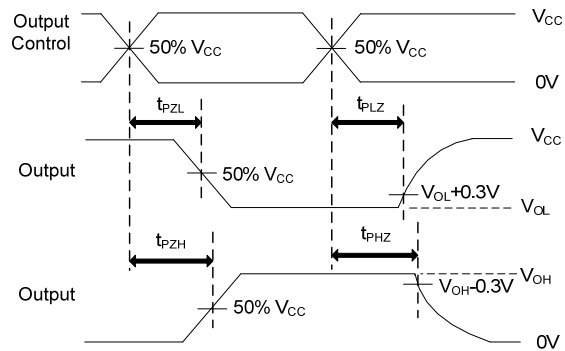
SETUP TIME AND HOLD TIME



PULSE WIDTH



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1MHz$, $Z_o = 50\Omega$,

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