



UPGE85N33

Preliminary

Insulated Gate Bipolar Transistor

WITH ANTI-PARAALLEL DIODE FOR PDP SUSTAIN CIRCUIT

■ DESCRIPTION

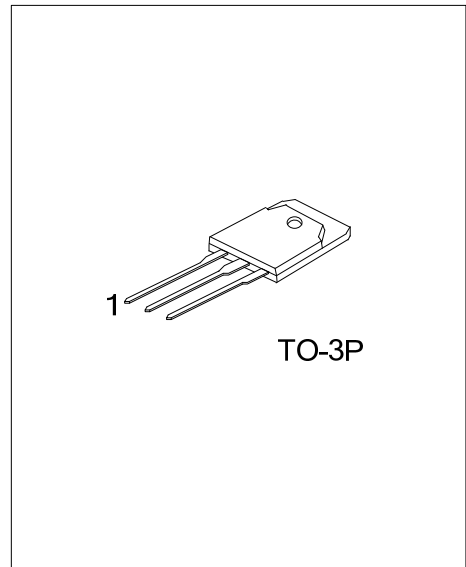
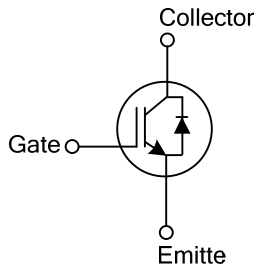
The UTC UPGE85N33 is with Anti-Parallel Diode for PDP Sustain Circuit. it uses UTC's advanced technology to provide customers with high input impedance, high switching speed and low conduction loss, etc.

The UTC UPGE85N33 is suitable for high voltage switching, high frequency switch mode power supplies.

■ FEATURES

- * $V_{CE(SAT)} \leq 1.9V @ I_C=50A, V_{GE}=15V$
- $V_{CE(SAT)} \leq 2.9V @ I_C=100A, V_{GE}=15V$
- * High switching speed
- * High input impedance
- * Low conduction loss

■ SYMBOL



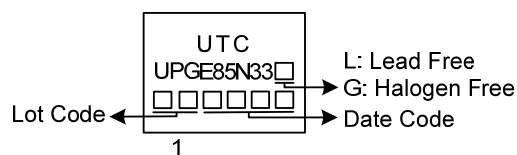
■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UPGE85N33L-T3P-T	UPGE85N33G-T3P-T	TO-3P	G	C	E	Tube

Note: Pin Assignment: A: Anode K: Cathode

<p>UPGE85N33G-T3P-T</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) T: Tube (2) T3P: TO-3P (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Collector-Emitter Voltage	V_{CES}	330	V
Gate to Emitter Voltage Continuous	V_{GES}	± 30	V
Continuous Collector Current	I_C	$T_C=25^\circ\text{C}$	170
		$T_C=100^\circ\text{C}$	85
Collector Current Pulsed (Note 2)	I_{CM}	240	A
Continuous Forward Current	I_F	$T_C=25^\circ\text{C}$	85
		$T_C=100^\circ\text{C}$	42.5
Forward Current Pulsed	I_{FM}	90	A
Peak Diode Recovery dv/dt (Note 3)	dv/dt	5.7	V/ns
Power Dissipation	P_D	150	W
Junction Temperature	T_J	$-55 \sim +150$	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	$-55 \sim +150$	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $I_F \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{CC} \leq BV_{CES}$, Starting $T_J=25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Case	θ_{JC}	0.83	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C=250\mu\text{A}$, $V_{GE}=0\text{V}$	330			V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE}=330\text{V}$, $V_{GE}=0\text{V}$			10	μA
Gate to Emitter Leakage Current	I_{GES}	$V_{CE}=0\text{V}$, $V_{GE}=\pm 20\text{V}$			± 100	nA
ON CHARACTERISTICS						
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C=50\text{A}$, $V_{GE}=15\text{V}$	$T_J=25^\circ\text{C}$		1.9	V
			$T_J=150^\circ\text{C}$		1.8	V
		$I_C=100\text{A}$, $V_{GE}=15\text{V}$	$T_J=25^\circ\text{C}$		2.9	V
			$T_J=150^\circ\text{C}$		2.6	V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C=250\mu\text{A}$, $V_{CE}=V_{GE}$	3.5		6.0	V
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{IES}	$V_{CE}=25\text{V}$, $V_{GE}=0\text{V}$, $f=1\text{MHz}$		1620		pF
Output Capacitance	C_{OES}			215		pF
Reverse Transfer Capacitance	C_{RES}			45		pF
SWITCHING CHARACTERISTICS						
Total Gate Charge	Q_G	$I_C=85\text{A}$, $V_{CE}=280\text{V}$, $V_{GE}=10\text{V}$		60		nC
Gate-Emitter Charge	Q_{GE}			15		nC
Gate-Collector Charge	Q_{GC}			28		nC
Current Turn-On Delay Time	$t_{D(ON)}$	$I_C=85\text{A}$, $V_{CE}=15\text{V}$, $V_{CE}=240\text{V}$, $R_G=25\Omega$		18		ns
Current Rise Time	t_R			25		ns
Current Turn-Off Delay Time	$t_{D(OFF)}$			170		ns
Current Fall Time	t_F			290		ns
DRAIN-SOURCE DIODE CHARACTERISTICS						
Forward Voltage Drop	V_{FM}	$I_F=85\text{A}$, $V_{GE}=0\text{V}$			2.5	V
Reverse Recovery Time	t_{rr}	$I_F=30\text{A}$, $di/dt=100\text{A}/\mu\text{s}$, $V_{CC}=100\text{V}$		65		ns
Reverse Recovery Charge	Q_{rr}			205		nC

Note: Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

■ TEST CIRCUIT AND WAVEFORMS

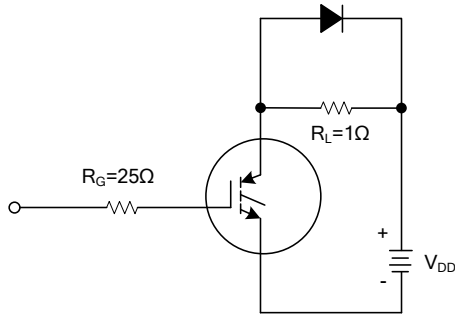


Fig 1. INDUCTIVE SWITCHING TEST CIRCUIT

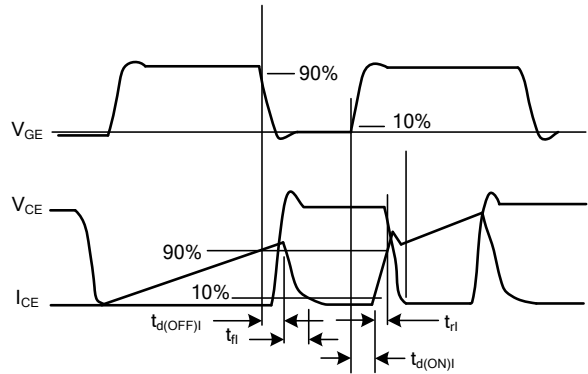


Fig 2. SWITCHING TEST WAVEFORMS

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