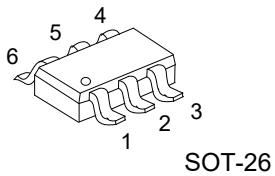
# THREE-RAIL SIMPLE POWER SEQUENCER



SOT-26

## ■ DESCRIPTION

The UTC **UPSS3880** simple power supply sequencer offers the easiest method to control power up sequencing and power down sequencing of multiple Independent voltage rails. By staggering the startup sequence, it is possible to avoid latch conditions or large in-rush currents that can affect the reliability of the system.

Available in a 6-pin SOT-26 package, the Simple Sequencer contains a precision enable pin and three open-drain output flags. The open-drain output flags permit that they can be pulled up to distinct voltage supplies separate from the sequencer $V_{DD}$ (so long as they do not exceed the recommended maximum voltage of 0.3V greater than $V_{DD}$), so as to interface with ICs requiring a range of different enable signals.

When the UTC **UPSS3880** is enabled, the three output flags will sequentially release, after individual time delays, thus permitting the connected power supplies to start up. The output flags will follow a reverse sequence during power down to avoid latch conditions.

## ■ FEATURES

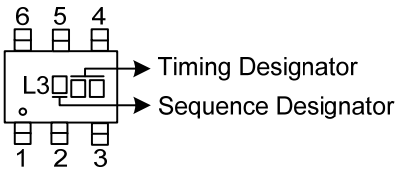
* Qualified for Automotive Applications
* Simple Solution for Sequencing 3 Voltage Rails from a Single Input Signal
* Power-Up and Power-Down Control
* Low Quiescent Current of 25μA
* Input Voltage Range of 3.3V to 5.5V
* Standard Timing Options Available

## ■ ORDERING INFORMATION

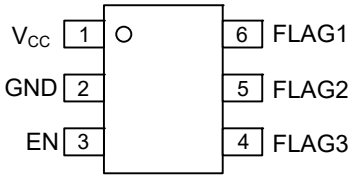
| Ordering Number | | Package | Packing |
|---|---|---|---|
| Lead Free | Halogen Free | | |
| UPSS3880L-AG6-xxx-R | UPSS3880G-AG6-xxx-R | SOT-26 | Tape Reel |

| | |
|---|---|
| UPSS3880G-AG6-xxx-R<br>(1)Packing Type<br>(2)Timing Designator<br>(3)Sequence Designator<br>(4)Package<br>(5)Green Package | (1) R: Tape Reel<br>(2) refer to Table 2.<br>(3) refer to Table 1.<br>(4) AG6: SOT-26<br>(5) G: Halogen Free and Lead Free, L: Lead Free |

## ■ MARKING




## ■ PIN CONFIGURATION




## ■ PIN DESCRIPTION

| PIN NO. | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{CC}$ | Input supply |
| 2 | GND | Ground |
| 3 | EN | Enable pin. |
| 4 | FLAG3 | Open-drain output 3 |
| 5 | FLAG2 | Open-drain output 2 |
| 6 | FLAG1 | Open-drain output 1 |

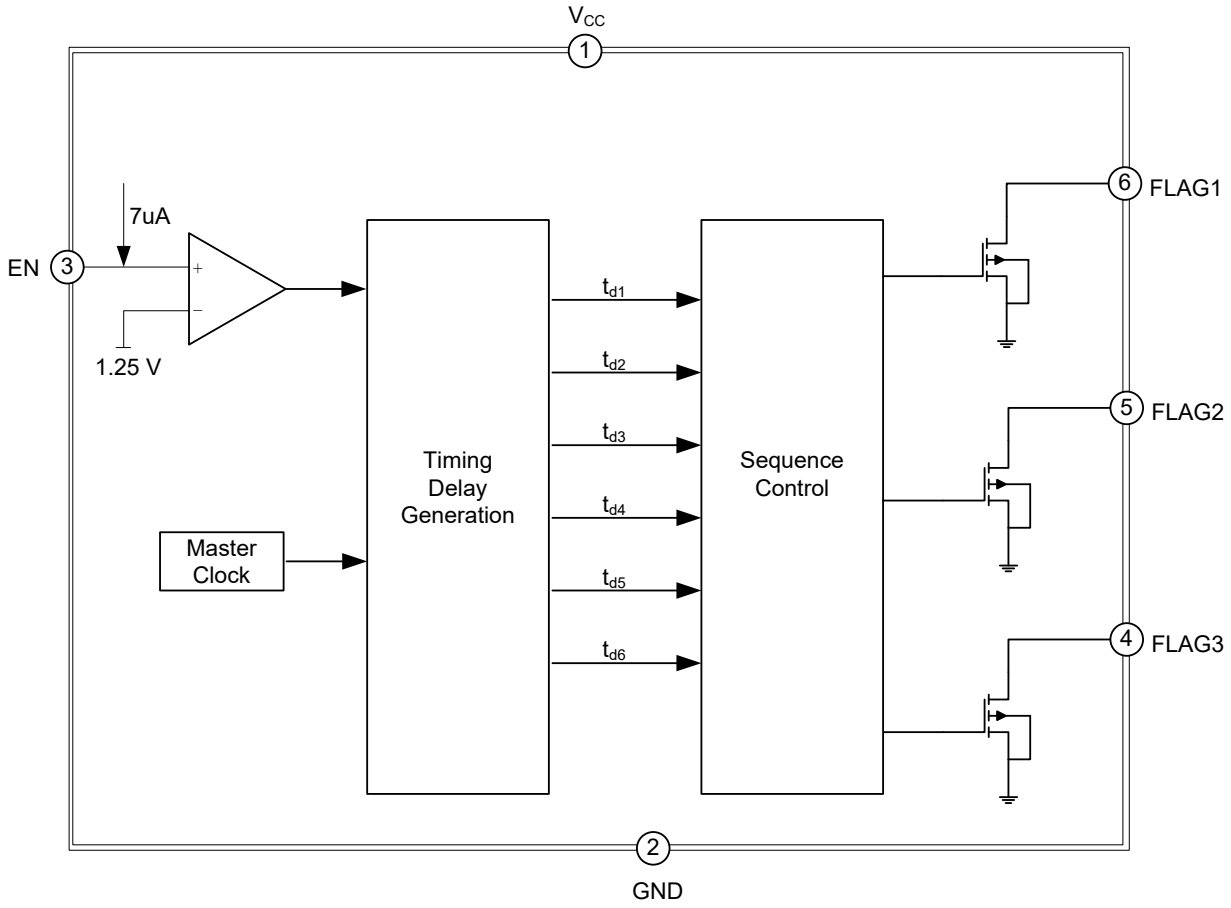
**Table 1. Sequence Designator Table**

| SEQUENCE NUMBER | FLAG ORDER | |
|---|---|---|
| | POWER UP | POWER DOWN |
| 1 | 1 - 2 - 3 | 3 - 2 - 1 |

**Table 2. Timing Designator Table**

| TIMING DESIGNATOR | $t_{d1}$ | $t_{d2}$ | $t_{d3}$ | $t_{d4}$ | $t_{d5}$ | $t_{d6}$ |
|---|---|---|---|---|---|---|
| AB | 30ms | 30ms | 30ms | 30ms | 30ms | 30ms |
| AC | 60ms | 60ms | 60ms | 60ms | 60ms | 60ms |
| AD | 120ms | 120ms | 120ms | 120ms | 120ms | 120ms |

## ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATING ($T_A$=25°C, unless otherwise specified)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Current | $V_{CC}$ | 6.0 | V |
| EN, FLAG1, FLAG2, FLAG3 | | 6.0 | V |
| Junction Temperature | $T_J$ | +150 | °C |
| Storage Temperature | $T_{STG}$ | -65 ~ +150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ RECOMMENDED OPERATING CONDITIONS ($T_A$=25°C, unless otherwise specified)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ to GND | 3.3 ~ 5.5 | V |
| EN, FLAG1, FLAG2, FLAG3 | | $V_{CC}$+0.3 | V |

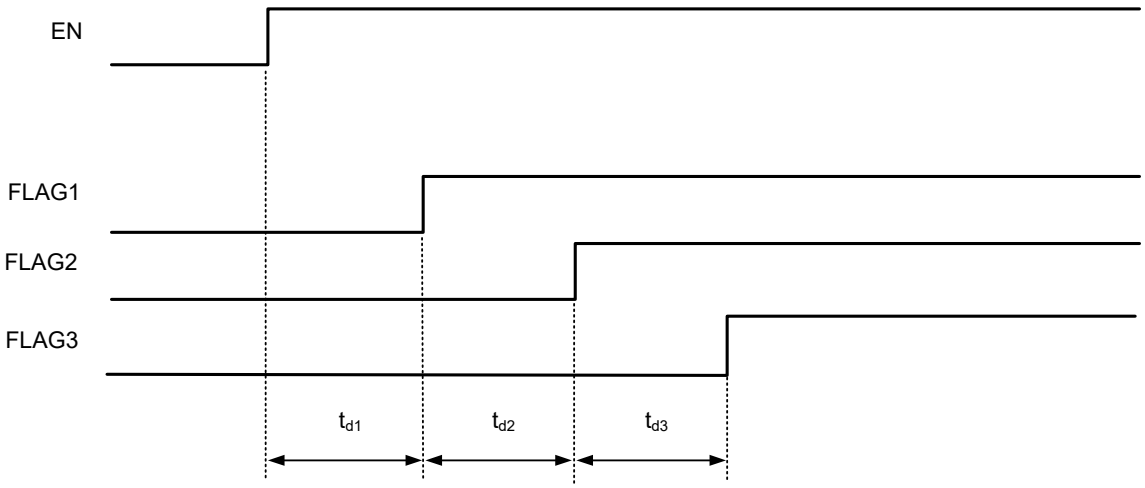
## ■ THERMAL DATA

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Junction to Ambient (Note 3) | $\theta_{JA}$ | 240 | °C/W |

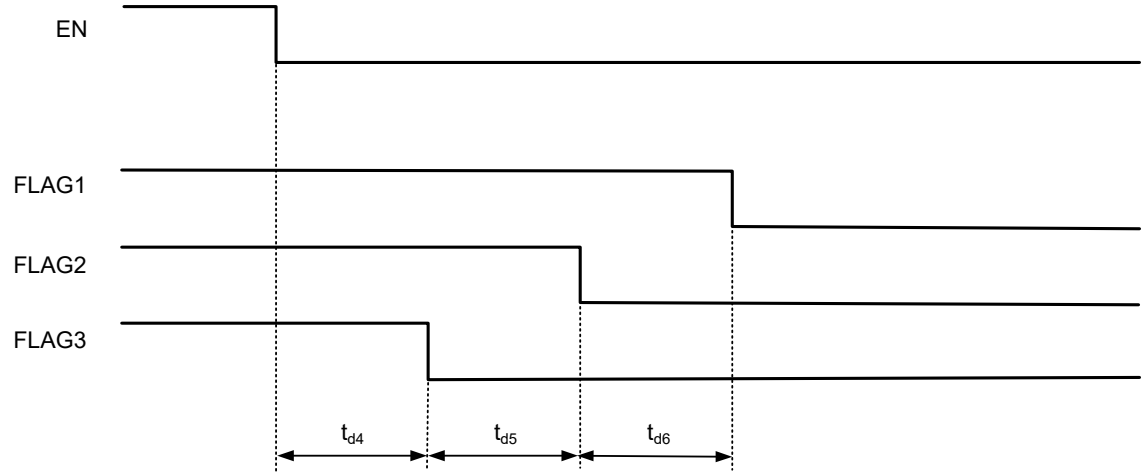
## ■ ELECTRICAL CHARACTERISTICS ($V_{DD}$=3.3V, $T_A$=25°C, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply Current (Quiescent) | $I_Q$ | | | 25 | 80 | μA |
| **OPEN-DRAIN FLAGS** | | | | | | |
| FLAGX Leakage Current | $I_{FLAG}$ | VFLAGX=3.3V | | 0.1 | 1 | μA |
| FLAGX Output Voltage Low | $V_{OL}$ | IFLAGX=1.2mA | | | 0.4 | V |
| **POWER-UP SEQUENCE** | | | | | | |
| Timer Delay 1 Accuracy | $t_{d1}$ | All Other Timing Options | -15 | | 15 | % |
| Timer Delay 2 Accuracy | $t_{d2}$ | All Other Timing Options | -15 | | 15 | % |
| Timer Delay 3 Accuracy | $t_{d3}$ | All Other Timing Options | -15 | | 15 | % |
| **POWER-DOWN SEQUENCE** | | | | | | |
| Timer Delay 4 Accuracy | $t_{d4}$ | All Other Timing Options | -15 | | 15 | % |
| Timer Delay 5 Accuracy | $t_{d5}$ | All Other Timing Options | -15 | | 15 | % |
| Timer Delay 6 Accuracy | $t_{d6}$ | All Other Timing Options | -15 | | 15 | % |
| **TIMING DELAY ERROR** | | | | | | |
| Ratio of Timing Delays | $(t_{d(x)}$-400μs) / $t_{d(x+1)}$ | For x=1 or 4 | 95 | | 105 | % |
| | $t_{d(x)}$ / $t_{d(x+1)}$ | For x=2 or 5 | 95 | | 105 | % |
| **ENABLE PIN** | | | | | | |
| EN Pin Threshold | $V_{EN}$ | | 1.0 | 1.25 | 1.4 | V |
| EN Pin Pull Up Current | $I_{EN}$ | $V_{EN}$=0V | | 7 | | μA |

## ■ TIMING DIAGRAMS




**Power-Up Sequence**




**Power-Down Sequence**

## ■ APPLICATION INFORMATION

The Simple Power Supply Sequencer contains three open-drain output flags which need to be pulled up for properoperation.100-kΩ resistors can be used as pull up resistors.

The Simple Power Supply Sequencer is used to implement a power-up and power-down sequence of three power supplies.

UTC **UPSS3880** has a power-up sequence (1 –2–3) and power-down sequence (3 –2–1).

## ■ DETAILED DESCRIPTION

**Overview**

The UTC **UPSS3880** simple power supply sequencer provides a simple solution for sequencing multiple rails in a controlled manner. Six independent timers are integrated to control the timing sequence (power up and power down) of three open-drain output flags. These flags permit connection to either a shutdown or enable pin of linear regulators and switchers to control the operation of the power supplies. This allows design of a complete power system without concern for large inrush currents or latch-up conditions that can occur.

The timing sequence of the device is controlled entirely by the enable (EN) pin. Upon power up, all the flags are held low until this precision enable is pulled high. When the EN pin is asserted, the power-up sequence starts. An internal counter delays the first flag (FLAG1) from rising until a fixed time period has expired. When the first flag is released, another timer will begin to delay the release of the second lag (FLAG2). This process repeats until all three flags have sequentially been released.

The power-down sequence is the same as power-up sequence, but in reverse. When the EN pin is deasserted a timer will begin that delays the third flag (FLAG3) from pulling low. The second and first flag will then follow in a sequential manner after their appropriate delays. The three timers that are used to control the power-down scheme can also be individually programmed and are completely independent of the power-up timers.

**Enable Control**

The timing sequence of the UTC **UPSS3880** is controlled by the assertion of the enable signal. The enable pin is designed with an internal comparator, referenced to a bandgap voltage (1.25V), to provide a precision threshold. This allows a delayed timing to be externally set using a capacitor or to start the sequencing based on a certain event, such as a line voltage reaching 90% of nominal. For an additional delayed sequence from the rail powering $V_{CC}$, simply attach a capacitor to the EN pin.

## ■ TYPICAL APPLICATION CIRCUIT