



ULM3086

Preliminary

NPN EPITAXIAL SILICON TRANSISTOR

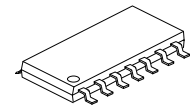
TRANSISTOR ARRAYS

DESCRIPTION

The UTC **ULM3086** each consists of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistor is well suited to a wide variety of applications in low power system in the DC through VHF range. It may be used as discrete transistors in conventional circuits however, in addition, it provides the very significant inherent integrated circuit advantages of close electrical and thermal matching.

FEATURES

- * Five general purpose monolithic transistors
- * Operation from DC to 120MHz
- * Wide operating current range



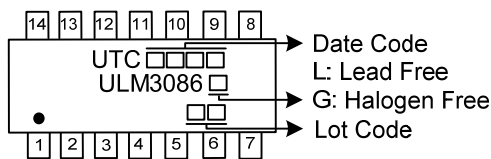
SOP-14

ORDERING INFORMATION

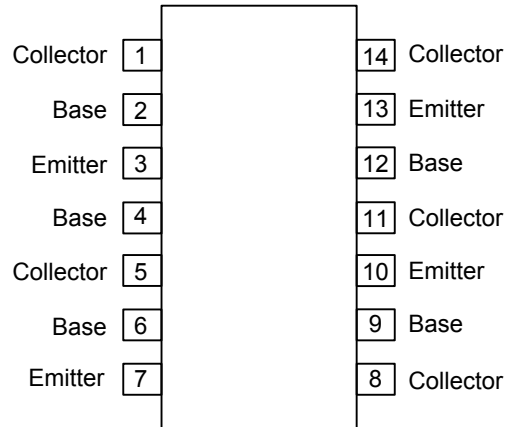
Ordering Number		Package	Packing
Lead Free	Halogen Free		
ULM3086L-S14-R	ULM3086G-S14-R	SOP-14	Tape Reel

<p>ULM3086G-S14-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) S14: SOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



■ PIN CONFIGURATION



■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Collector to Emitter Voltage	V_{CEO}	15	V
Collector to Base Voltage	V_{CBO}	20	V
Collector to Substrate Voltage (Note 1)	V_{CIO}	20	V
Emitter to Base Voltage	V_{EBO}	5	V
Collector Current	I_C	50	mA
Power Dissipation	P_D	750	mW
Operating Temperature Range	T_{OPR}	-40 ~ +85	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-65 ~ +85	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

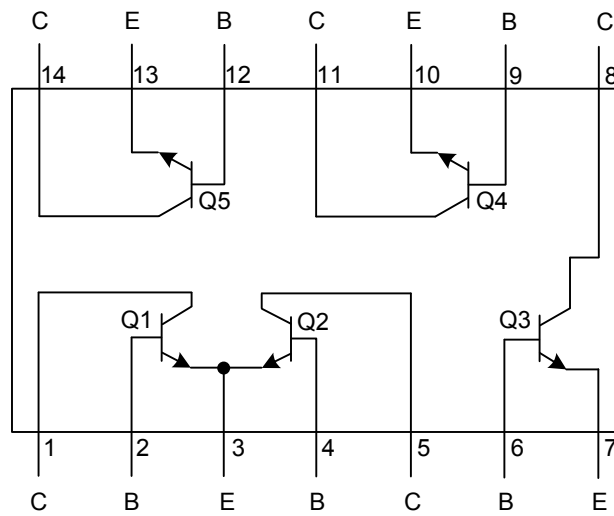
2. The collector of each transistor of the UTC **ULM3086** is isolated from the substrate by an integral diode.

The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action..

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C=10\mu\text{A}$, $I_E=0$	20	60		V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C=1\text{mA}$, $I_B=0$	15	24		V
Collector to Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C=10\mu\text{A}$, $I_{CI}=0$	20	60		V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E=10\mu\text{A}$, $I_C=0$	5	7		V
Collector Cutoff Current	I_{CBO}	$V_{CB}=10\text{V}$, $I_E=0$		0.002	100	nA
Collector Cutoff Current	I_{CEO}	$V_{CE}=10\text{V}$, $I_B=0$			5	μA
Static Forward Current Transfer Ratio (Static Beta)	h_{FE}	$V_{CE}=3\text{V}$	$I_C=10\text{mA}$		100	
			$I_C=1\text{mA}$	40	100	
			$I_C=10\mu\text{A}$		54	
Base to Emitter Voltage	V_{BE}	$V_{CE}=3\text{V}$	$I_E=1\text{mA}$		0.715	V
			$I_E=10\text{mA}$		0.800	V
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_B=1\text{mA}$, $I_C=10\text{mA}$		0.23		V
Low Frequency Noise Figure	NF	$f=1\text{kHz}$, $V_{CE}=3\text{V}$, $I_C=100\mu\text{A}$, $R_S=1\text{k}\Omega$		3.25		dB

■ SCHEMATIC AND CONNECTION DIAGRAM



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