UCA82C251 **CMOS IC** 

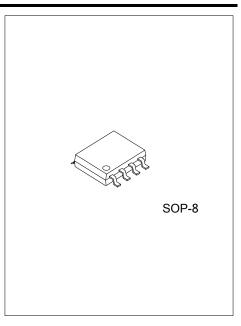
# **CAN TRANSCEIVER FOR 24V SYSTEMS**

#### DESCRIPTION

The UTC UCA82C251 is the interface between a CAN protocol controller and the physical bus. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller. It is primarily intended for applications up to 1 MBd in trucks and buses.

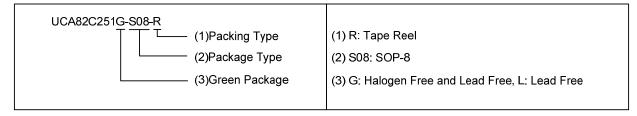
#### **FEATURES**

- \* Fully compatible with the "ISO 11898-24V" standard
- \* Slope control to reduce Radio Frequency Interference (RFI)
- \* Short-circuit proof to battery and ground in 24V powered systems
- \* An unpowered node does not disturb the bus lines
- \* Thermally protected
- \* Low-current Standby mode
- \* At least 110 nodes can be connected
- \* High speed (up to 1 MBd)
- \* High immunity against electromagnetic interference

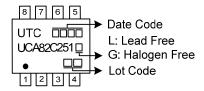


#### ORDERING INFORMATION

Ordering	Number	Doolsono	Packing	
Lead Free	Halogen Free	Package		
UCA82C251L-S08-R	UCA82C251G-S08-R	SOP-8	Tape Reel	

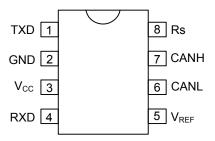


#### **MARKING**



www.unisonic.com.tw 1 of 9 QW-R140-037.D

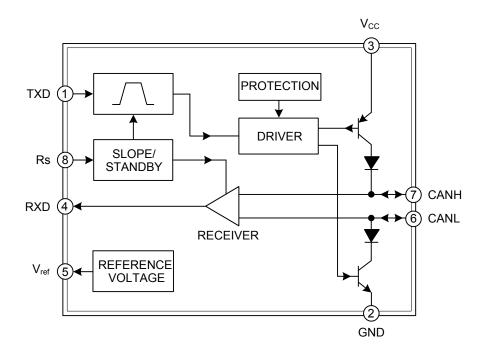
## ■ PIN CONFIGURATION



## ■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION	
1	TXD	Transmit data input	
2	GND	Ground	
3	V <sub>CC</sub>	Supply voltage	
4	RXD	Receive data output	
5	$V_{REF}$	Reference voltage output	
6	CANL	LOW-level CAN voltage input/output	
7	CANH	HIGH-level CAN voltage input/output	
8	Rs	Slope resistor input	

## ■ BLOCK DIAGRAM



#### **■ ABSOLUTE MAXIMUM RATING**

PARAMETE	:R	SYMBOL	RATINGS	UNIT
Supply Voltage		$V_{CC}$	-0.3 ~ +7.0	V
DC Voltage at Pins 1, 4, 5 and 8		Vn	-0.3 ~ V <sub>CC</sub> +0.3	V
	0V < V <sub>CC</sub> < 5.5V, TXD HIGH or Floating		-36 ~ +36	٧
DC Voltage at Pin 6 (CANL)	0V < V <sub>CC</sub> < 5.5V, no time limit (Note 1)	V <sub>6</sub>	-36 ~ +36	V
	0V < V <sub>CC</sub> < 5.5V, no time limit (Note 2)		-36 ∼+36	V
DC Voltage at Pin 7 (CANH) 0V < V <sub>CC</sub> < 5.5V, no time limit		V <sub>7</sub>	-36 ∼+36	V
Transient Voltage at Pins 6 and 7 see Figure 6		$V_{TRT}$	-200 ~ +200	٧
Ambient Temperature		T <sub>A</sub>	-40 ~ +125	°C
Junction Temperature		$T_J$	+150	°C
Storage Temperature		$T_{STG}$	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

#### **■ THERMAL DATA**

PARAMETER		SYMBOL	RATINGS	UNIT
Thermal Resistance from Junction to Ambient	In Free Air	$\theta_{JA}$	160	K/W

## **■ ELECTRICAL CHARACTERISTICS**

 $V_{CC}$ = 4.5V~5.5V;  $T_A$ =-40°C~+125°C;  $R_L$ =60 $\Omega$ ;  $I_8$ >-10 $\mu$ A; unless otherwise specified; all voltages referenced to ground (Pin 2); positive input current; all parameters are guaranteed over the ambient temperature range by design, but only 100 % tested at +25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	NAINI	TVD	MAN	UNIT
	STIMBUL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
		Dominant, V₁=1V, V <sub>CC</sub> =5.1V			78	mΑ
		Dominant, V <sub>1</sub> =1V, V <sub>CC</sub> =5.25V			80	mA
Supply Current	l <sub>3</sub>	Dominant, V <sub>1</sub> =1V, V <sub>CC</sub> =5.5V			85	mA
		Recessive, $V_1$ =4 $V$ , $R_8$ =47 $k\Omega$			12	mΑ
		Standby (Note 1)			330	μΑ
DC BUS TRANSMITTER						
HIGH-Level Input Voltage	V <sub>IH</sub>	Output Recessive	0.7×V <sub>CC</sub>		V <sub>CC</sub> +0.3	V
LOW-Level Input Voltage	$V_{IL}$	Output Dominant	-0.3		0.3×V <sub>CC</sub>	V
HIGH-Level Input Current	I <sub>IH</sub>	V <sub>1</sub> =4V	-200		+30	μΑ
LOW-Level Input Current	I <sub>IL</sub>	V <sub>1</sub> =1V	-100		-600	μΑ
Recessive Bus Voltage	V <sub>6,7</sub>	V₁=4V, No Load	2.0		3.0	V
CANILL Output Maltage	\/_	V <sub>1</sub> =1V, V <sub>CC</sub> =4.75V ~ 5.5V	3.0		4.5	V
CANH Output Voltage	V <sub>7</sub>	V <sub>1</sub> =1V, V <sub>CC</sub> =4.5V ~ 4.75V	2.75		4.5	V
CANL Output Voltage	$V_6$	V <sub>1</sub> =1V	0.5		2.0	V
Difference Between Output Voltage at Pins 6 and 7	ΔV <sub>6, 7</sub>	V <sub>1</sub> =1V	1.5		3.0	V
		$V_1$ =1V, $R_L$ =45 $\Omega$	1.5			V
		V <sub>1</sub> =4V, No Load	-500		+50	mV
01 10: "01	I <sub>sc7</sub>	V <sub>7</sub> =-5V			-200	mA
Short-Circuit CANH Current		V <sub>7</sub> =-30V		-100		mA
Short-Circuit CANL Current	I <sub>sc6</sub>	V <sub>6</sub> =36V			200	mA

<sup>2.</sup> TXD is LOW. Short-circuit protection provided for slew rates up to 5V/  $\mu$  s for voltages above +30V.

## **CMOS IC**

## **■ ELECTRICAL CHARACTERISTICS (Cont.)**

Differential Input Voltage (Recessive)   V_DIFF(IV)	PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ \begin{array}{c} (Recessive) & V_{DIFF(I)} \\ (Recessive) & V_{DIFF(I)} \\ (Dominant) $	DC BUS RECEIVER: V <sub>1</sub> = 4V; PINS 6 AND 7 EXTERNALLY DRIVEN; -2V<(V <sub>6</sub> , V <sub>7</sub> ) < 7V; UNLESS OTHERWISE SPECIFIED						
1.0   1.0	Differential Input Voltage	\/	Note 2	-1.0		+0.5	V
Differential Input Voltage (Dominant)   V_DIFF(d)   Standby Mode   1.0   5.0   V   Standby Mode   Standby Mode   0.97   5.0   V   Standby Mode   0.97   5.0   V   Standby Mode   V_DIFF(mys)   Standby Mode   V_CC=4.5V ~ 5.10V   0.91   5.0   V   V   V   V   V   V   V   V   V	(Recessive)	V DIFF(r)	-7V<(V <sub>6</sub> ,V <sub>7</sub> ) < 12V (Note 2)	-1.0		+0.4	V
Standby Mode   0.97   5.0   V				0.9		5.0	V
Standby Mode   V <sub>CC</sub> =4.5V ~ 5.10V   0.91   5.0   V	Differential Input Voltage	17	$-7V < (V_6, V_7) < 12 V$ ; not Standby Mode	1.0		5.0	V
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	(Dominant)	V DIFF(d)	Standby Mode	0.97		5.0	V
HIGH-Level Output Voltage VoH pin 4, $I_a$ = -100μA			Standby Mode, V <sub>CC</sub> =4.5V ~ 5.10V	0.91		5.0	V
	Differential Input Hysteresis	$V_{DIFF(hys)}$	see Figure 3		150		mV
LOW-Level Output Voltage $V_{OL}$ $I_{Ia}$ =10mA $0$ $1.5$ $V$ Input Resistance $R_{II}$ CANH, CANL $1$ $1.5$	HIGH-Level Output Voltage		pin 4, I <sub>4</sub> = -100μA	0.8×V <sub>CC</sub>		$V_{CC}$	V
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	LOW Love Output Voltage	\/	pin 4, I <sub>4</sub> =1mA	0		$0.2\ V_{CC}$	V
Differential Input Resistance $R_{DIFF}$ 20100 $K\Omega$ Reference outputReference Output Voltage $V_{REF}$ $V_{8}=1V$ , $ I_{5}  < 50\mu A$ $0.45\times V_{CC}$ $0.55\times V_{CC}$ $V$ Reference Output Voltage $V_{REF}$ $V_{8}=1V$ , $ I_{5}  < 50\mu A$ $0.45\times V_{CC}$ $0.55\times V_{CC}$ $V$ TIMING ( $C_{L}$ =100PF; SEE FIGURE 1, FIGURE 2, FIGURE 4 AND FIGURE 5)Delay TXD to Bus Active $t_{ON_{LXD}}$ $R_{EXT}=0\Omega$ <t< td=""><td>LOW-Level Output Voltage</td><td>V<sub>OL</sub></td><td>I<sub>4</sub>=10mA</td><td>0</td><td></td><td>1.5</td><td>V</td></t<>	LOW-Level Output Voltage	V <sub>OL</sub>	I <sub>4</sub> =10mA	0		1.5	V
Reference Output Voltage $V_{REF}$ $V_8=1V, \mid I_5\mid <50\mu A$ $0.45\times V_{CC}$ $0.55\times V_{CC}$ $V$ $0.6\times V_{CC}$ $V$	Input Resistance	$R_{i}$	CANH, CANL	5		25	kΩ
Reference Output Voltage $V_{REF} = \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Differential Input Resistance	R <sub>DIFF</sub>		20		100	kΩ
Reference Output Voltage $V_{REF}$ $V_8=4V, \mid I_5\mid <5\mu A$ $0.4\times V_{CC}$ $0.6\times V_{CC}$ $V$ TIMING ( $C_L=100PF;$ SEE FIGURE 1, FIGURE 2, FIGURE 4 AND FIGURE 5)  Delay TXD to Bus Active $I_{ON, TXD}$ $R_{EXT}=0\Omega$ $I_{OSM}$ $I_{$	Reference output						
TIMING (C <sub>L</sub> =100PF; SEE FIGURE 1, FIGURE 2, FIGURE 4 AND FIGURE 5)  Delay TXD to Bus Active $t_{ON, TXD}$ $R_{EXT}=0\Omega$ $t_{OFF, TXD}$	Deference Output Valtage	.,	V <sub>8</sub> =1V,   I <sub>5</sub>   <50μA	0.45×V <sub>cc</sub>		0.55×V <sub>CC</sub>	V
Delay TXD to Bus Active $t_{ON,TXD}$ $R_{EXT}=0\Omega$ nsDelay TXD to Bus Inactive $t_{OFF,TXD}$ $R_{EXT}=0\Omega$ 40nsDelay TXD to Receiver Active $t_{ON,RXD}$ $R_{EXT}=0\Omega$ 55nsDelay TXD to Receiver Inactive $t_{OFF,RXD}$ $R_{EXT}=0\Omega$ , $T_A<+85^{\circ}C$ , $V_{CC}=4.5V \sim 5.1V$ 80ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V \sim 5.1V$ 80170ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V \sim 5.1V$ 80170ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V \sim 5.1V$ 90170ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V \sim 5.1V$ 90190ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V \sim 5.1V$ 90190ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V \sim 5.1V$ 90190ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V \sim 5.1V$ 90170ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V \sim 5.1V$ 80170ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V \sim 5.1V$ 80170ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V \sim 5.1V$ 90170ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V \sim 5.1V$ 40550ns $R_{EXT}=0\Omega$ , $R_{EXT}=47K\Omega$ 7 $V/\mu$ $V/$	Reference Output Voltage	<b>V</b> REF	V <sub>8</sub> =4V,   I <sub>5</sub>   <5µA	0.4×V <sub>CC</sub>		0.6×V <sub>CC</sub>	V
Delay TXD to Bus Inactive Delay TXD to Receiver Active $t_{OFF\_TXD}$ $t_{ON\_RXD}$ $R_{EXT}=0\Omega$ 40nsDelay TXD to Receiver Inactive $t_{ON\_RXD}$ $R_{EXT}=0\Omega$ 55nsDelay TXD to Receiver Inactive $t_{OFF\_RXD}$ $R_{EXT}=0\Omega$ , $V_{CC}=4.5V\sim5.1V$ 80ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V\sim5.1V$ 80170ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V\sim5.1V$ 80170ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V\sim5.1V$ 80170ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V\sim5.1V$ 80170ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V\sim5.1V$ 90170ns $R_{EXT}=0\Omega$ , $V_{CC}=4.5V\sim5.1V$ 400ns $R_{EXT}=0\Omega$ , $V_{CC}=$	TIMING (CL=100PF; SEE FIGURE	JRE 1, FIC	SURE 2, FIGURE 4 AND FIGURE 5)				
Delay TXD to Receiver Active $t_{ON\_RXD}$ $R_{EXT}=0\Omega$ $S55$ $ns$ $R_{EXT}=0\Omega$ , $T_{A}<+85^{\circ}C$ , $T_$	Delay TXD to Bus Active	$t_{ON\_TXD}$	$R_{EXT}$ =0 $\Omega$				ns
Delay TXD to Receiver Inactive $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Delay TXD to Bus Inactive	t <sub>OFF_TXD</sub>	$R_{EXT}$ =0 $\Omega$		40		ns
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Delay TXD to Receiver Active	$t_{ON\_RXD}$	$R_{EXT}$ =0 $\Omega$		55		ns
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			$R_{EXT}=0\Omega$ , $T_A<+85^{\circ}C$ , $V_{CC}=4.5V \sim 5.1V$		80		ns
Inactive $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Dalay TVD to Dagaiyar	t <sub>OFF_RXD</sub>	$R_{EXT}$ =0 $\Omega$ , $V_{CC}$ = 4.5 $V \sim 5.1V$		80	170	ns
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	-		$R_{EXT}=0\Omega$ , $T_A<+85^{\circ}C$		90	170	ns
Delay TXD to Receiver Active $t_{ON\_RXD}$ $R_{EXT}$ =47kΩ       440       550       ns         CANH, CANL Slew Rate $ SR $ $R_{EXT}$ =47kΩ       7 $V/\mu s$ Wake-Up Time from Standby (Via Pin 8) $t_{WAKE}$ see Figure 4       20 $\mu s$ Bus Dominant to RXD LOW $t_{D\_RXDL}$ $V_8$ =4V, see Figure 5       3 $\mu s$ STANDBY/SLOPE CONTROL (PIN 8)       Input Voltage for Standby Mode $V_{STB}$ 0.75× $V_{CC}$ $V_{CC}$ Slope Control Mode Current $I_{SLOPE}$ -10       -450 $\mu A$	lilactive		$R_{EXT}$ =0k $\Omega$		90	190	ns
CANH, CANL Slew Rate $ SR $ $R_{EXT}$ =47k $\Omega$ 7 $V/\mu s$ Wake-Up Time from Standby (Via Pin 8) $t_{WAKE}$ see Figure 4 $20$ $\mu s$ Bus Dominant to RXD LOW $t_{D_RXDL}$ $V_8$ =4V, see Figure 5 $3$ $\mu s$ STANDBY/SLOPE CONTROL (PIN 8) Input Voltage for Standby Mode $V_{STB}$ $0.75 \times V_{CC}$ $V$ Slope Control Mode Current $I_{SLOPE}$ $-10$ $-450$ $\mu A$			$R_{EXT}$ =47k $\Omega$		290	400	ns
Wake-Up Time from Standby (Via Pin 8) $t_{WAKE}$ see Figure 4 $20$ $\mu s$ Bus Dominant to RXD LOW $t_{D\_RXDL}$ $V_8$ =4V, see Figure 5 $3$ $\mu s$ STANDBY/SLOPE CONTROL (PIN 8)  Input Voltage for Standby $V_{STB}$ $0.75 \times V_{CC}$ $V$ Slope Control Mode Current $I_{SLOPE}$ $-10$ $-450$ $\mu A$	Delay TXD to Receiver Active	$t_{ON\_RXD}$	$R_{EXT}$ =47k $\Omega$		440	550	ns
	CANH, CANL Slew Rate	SR	$R_{EXT}$ =47k $\Omega$		7		V/µs
	Wake-Up Time from Standby	4	and Figure 4			20	
STANDBY/SLOPE CONTROL (PIN 8)           Input Voltage for Standby Mode         V <sub>STB</sub> 0.75×V <sub>CC</sub> V           Slope Control Mode Current         I <sub>SLOPE</sub> -10         -450         μA	(Via Pin 8)	lWAKE	see Figure 4			20	μs
Input Voltage for Standby $V_{STB}$ $0.75 \times V_{CC}$ $V$ Slope Control Mode Current $I_{SLOPE}$ $-10$ $-450$ $\mu A$	Bus Dominant to RXD LOW		V <sub>8</sub> =4V, see Figure 5			3	μs
Mode $V_{STB}$ $0.75 \times V_{CC}$ $V$ Slope Control Mode Current $I_{SLOPE}$ $-10$ $-450$ $\mu A$							
	Input Voltage for Standby Mode	$V_{\text{STB}}$		0.75×V <sub>CC</sub>			V
Slope Control Mode Voltage V <sub>SLOPE</sub> 0.4×V <sub>CC</sub> 0.6×V <sub>CC</sub> V	Slope Control Mode Current	I <sub>SLOPE</sub>		-10	_	-450	μĀ
	Slope Control Mode Voltage	$V_{SLOPE}$		0.4×V <sub>CC</sub>		$0.6 \times V_{CC}$	V

Notes: 1.  $I_1 = I_4 = I_5 = 0$ mA, 0V <  $V_6 < V_{CC}$ , 0V <  $V_7 < V_{CC}$ ,  $V_8 = V_{CC}$ ,  $T_A < 90$ °C.

<sup>2.</sup> This is valid for the receiver in all modes: High-speed, Slope control and Standby.

#### ■ FUNCTIONAL DESCRIPTION

The UTC **UCA82C251** is the interface between a CAN protocol controller and the physical bus. It is primarily intended for applications up to 1 MBd in trucks and buses. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller. It is fully compatible with the "ISO 11898-24 V" standard.

A current-limiting circuit protects the transmitter output stage against short-circuits to positive and negative battery voltage. Although power dissipation will increase as a result of a short circuit fault condition, this feature will prevent destruction of the transmitter output stage.

If the junction temperature exceeds approximately 160°C, the limiting current of both transmitter outputs is decreased. Because the transmitter is responsible for most of the power dissipated, this will result in reduced power dissipation and hence a lower chip temperature. All other parts of the IC will remain operational. The thermal protection is needed, in particular, when a bus line is short-circuited.

The CANH and CANL lines are also protected against electrical transients which may occur in an automotive environment.

Pin 8 (Rs) allows three different modes of operation to be selected: High-speed, Slope control and Standby.

For high-speed operation, the transmitter output transistors are simply switched on and off as fast as possible. In this mode, no measures are taken to limit the rise and fall slopes. A shielded cable is recommended to avoid RFI problems. High-speed mode is selected by connecting pin 8 to ground.

Slope control mode allows the use of an unshielded twisted pair or a parallel pair of wires as bus lines. To reduce RFI, the rise and fall slopes should be limited. The rise and fall slopes can be programmed with a resistor connected from pin 8 to ground. The slope is proportional to the current output at pin 8.

If a HIGH level is applied to pin 8, the circuit enters a low-current Standby mode. In this mode, the transmitter is switched off and the receiver is switched to a low current. If dominant bits are detected (differential bus voltage >0.9 V), RXD will be switched to a LOW level. The microcontroller should react to this condition by switching the transceiver back to normal operation (via pin 8). Because the receiver is slower in Standby mode, the first message will be lost at higher bit rates.

TXD **RXD** Supply CANH CANL Bus state 4.5V to 5.5V 0 HIGH LOW 0 dominant 1 (or Floating) 4.5V to 5.5V Floating Floating Recessive 1 (Note 1)  $4.5V < V_{CC} < 5.5V$ X (Note 2) Floating If Floating If Floating X (Note 1)  $0V < V_{CC} < 4.5V$ Floating Floating Floating Floating X (Note 2)

Table 1. Truth table of the CAN transceiver

Table 2. Pin Rs summary

Condition Forced at Pin Rs	Mode	Resulting Voltage or Current at Pin Rs
$V_{Rs} > 0.75 \times V_{CC}$	Standby	-I <sub>Rs</sub> < 10μA
10μA < -I <sub>Rs</sub> < 200μA	Slope Control	$0.4V_{CC} < V_{Rs} < 0.6 \times V_{CC}$
$V_{Rs} < 0.3V_{CC}$	High-Speed	-I <sub>Rs</sub> < 500μA

Notes: 1. If another bus node is transmitting a dominant bit, then RXD is logic 0.

<sup>2.</sup> X = don't care.

## **■ TEST CIRCUIT**

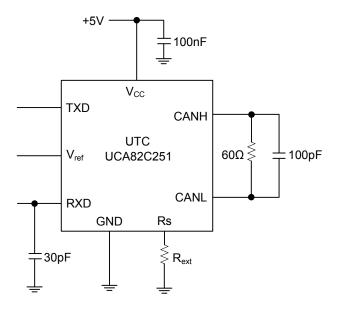


Figure 1. Test circuit for dynamic characteristics.

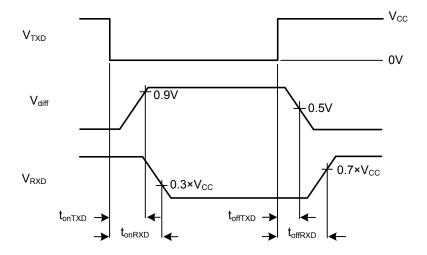


Figure 2. Timing diagram for dynamic characteristics.

## ■ TEST CIRCUIT (Cont.)

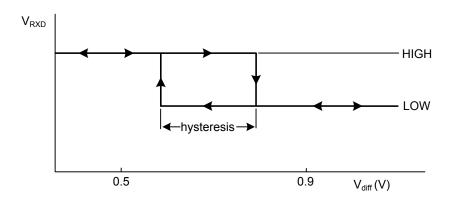


Figure 3. Hysteresis.

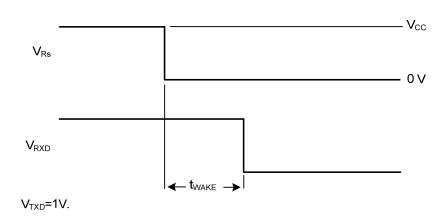


Figure 4. Timing diagram for wake-up from Standby.

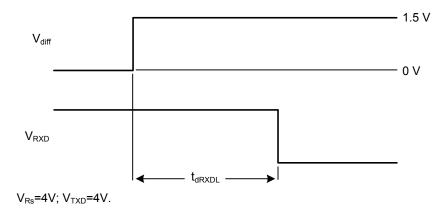
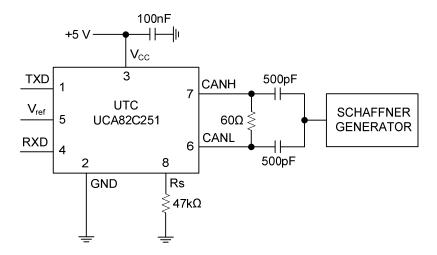


Figure 5. Timing diagram for bus dominant to RXD LOW.

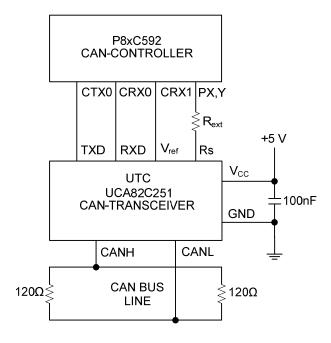
## ■ TEST CIRCUIT (Cont.)



The waveforms of the applied transients shall be in accordance with "ISO 7637 part 1", test pulses 1, 2, 3a and 3b.

Figure 6. Test circuit for automotive transients.

## **■ TYPICAL APPLICATION CIRCUIT**



- (1) The output control register of the P8xC592 should be programmed to 1AH (push-pull operation, dominant = LOW).
- (2) If no slope control is desired: Rext =0.

Figure 7. UTC UCA82C251 CAN transceiver application diagram

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**CMOS IC**