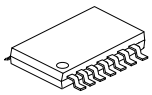
UNTS0104 **Preliminary** ***CMOS IC***

DUAL SUPPLY TRANSLATING TRANSCEIVER, OPEN DRAIN, AUTO DIRECTION SENSING



TSSOP-14

■ DESCRIPTION

The **UNTS0104** is a 4-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 4-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins (V_{CCA} and V_{CCB}), V_{CCA} can be supplied at any voltage between 1.65 V and 3.6 V and V_{CCB} can be supplied at any voltage between 2.3 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins An and OE are referenced to V_{CCA} and pins Bn are referenced to V_{CCB}, A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using IOFF. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

■ FEATURES

* 1.65V to 3.6V on A Port and 2.3 V to 5.5V on B Port
* I_{OFF} circuitry provides partial Power-down mode operation
* Inputs accept voltages up to 5.5V

■ APPLICATION

* I^2C/SMBus
* UART
* GPIO

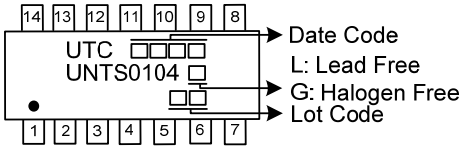
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UNTS0104L-P14-R	UNTS0104G-P14-R	TSSOP-14	Tape Reel

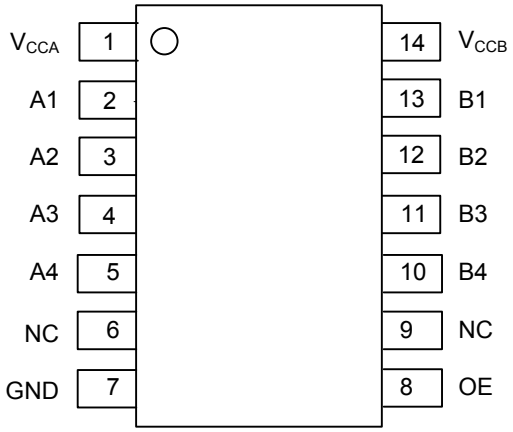
UNTS0104G-P14-R
- (1)Packing Type
- (2) Package Type
- (3) Green Package

(1) R: Tape Reel
(2) P14: TSSOP-14
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	DESCRIPTION
1	V_{CCA}		A-port supply voltage 1.65V ≤ V_{CCA} ≤ 3.6V and V_{CCA} ≤ V_{CCB}.
2	A1	I/O	Input/output 1. Referenced to V_{CCA}
3	A2	I/O	Input/output 2. Referenced to V_{CCA}
4	A3	I/O	Input/output 3. Referenced to V_{CCA}
5	A4	I/O	Input/output 4. Referenced to V_{CCA}
6	NC		No connection. Not internally connected.
7	GND		Ground
8	OE	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}
9	NC		No connection. Not internally connected.
10	B4	I/O	Input/output 4. Referenced to V_{CCB}
11	B3	I/O	Input/output 3. Referenced to V_{CCB}
12	B2	I/O	Input/output 2. Referenced to V_{CCB}
13	B1	I/O	Input/output 1. Referenced to V_{CCB}
14	V_{CCB}		B-port supply voltage 2.3V ≤ V_{CCB} ≤ 5.5V

Note: I=Input, I/O=Input and Output.

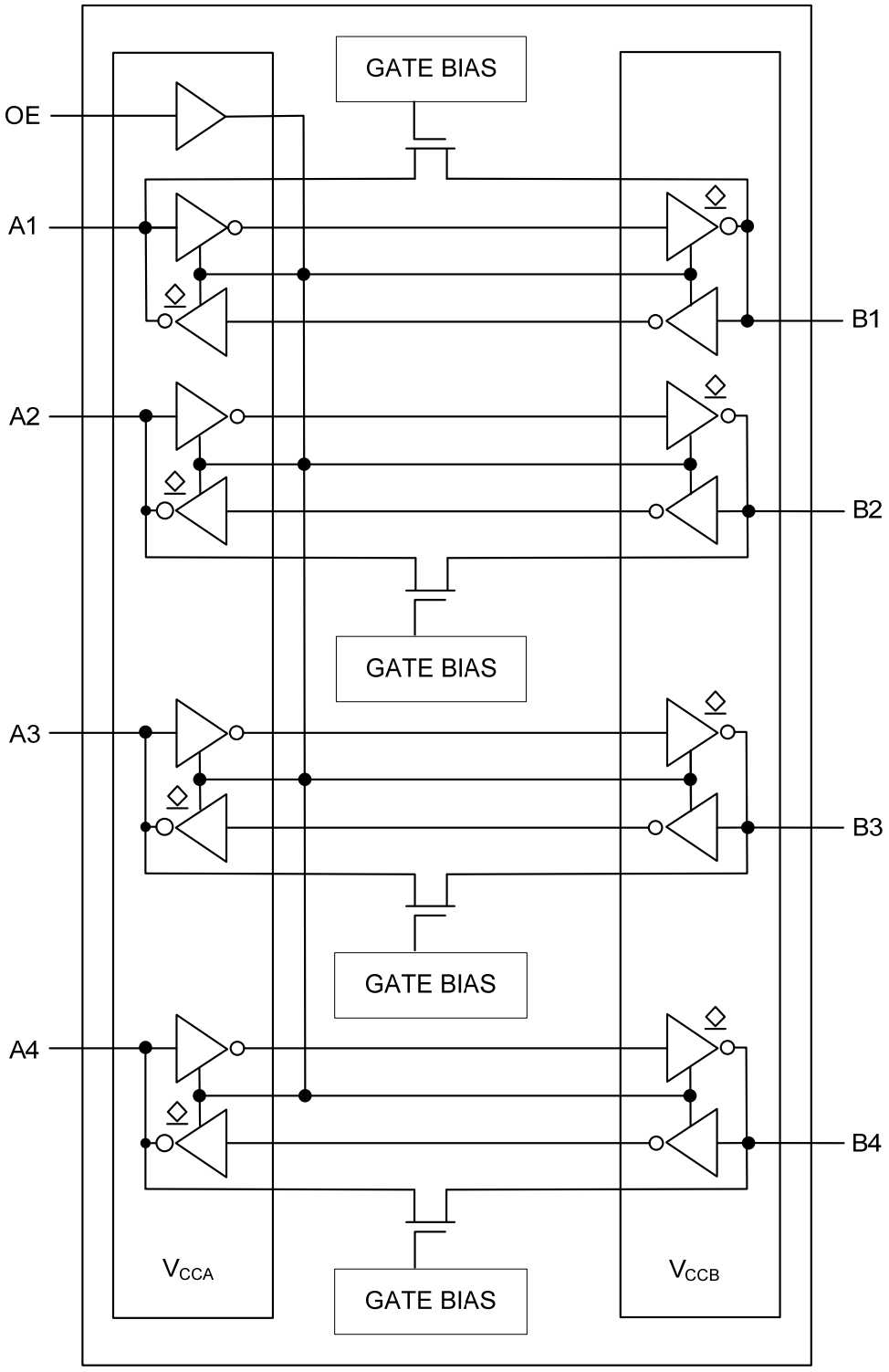
■ FUNCTION TABLE

SUPPLY VOLTAGE		INPUT	INPUT/OUTPUT	
V_{CCA}	V_{CCB}	OE	An	Bn
1.65V ~ V_{CCB}	2.3V ~ 5.5V	L	Z	Z
1.65V ~ V_{CCB}	2.3V ~ 5.5V	H	Input or Output	Output or Input
GND	GND	X	Z	Z

Notes: 1. H = High voltage level；L = Low voltage level；X = Don't care；Z = high-impedance OFF-state

2. When either V_{CCA} or V_{CCB} is at GND level, the device goes into power-down mode.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER			SYMBOL	RATINGS	UNIT
Supply Voltage			V_{CCA}	-0.5 ~ 6.5	V
Supply Voltage			V_{CCB}	-0.5 ~ 6.5	V
Input Voltage		A Port, OE Input	V_{IN}	-0.5 ~ 6.5	V
		B Port		-0.5 ~ 6.5	V
Output Voltage	Active mode	A or B Port	V_{OUT}	-0.5 ~ V_{CCO}+0.5	V
	Power-down or 3-state mode	A Port		-0.5 ~ 4.6	V
		B Port		-0.5 ~ 6.5	V
Input Clamp Current		V_{IN}<0V	I_{IK}	-50	mA
Output Clamp Current		V_{OUT}<0V	I_{OK}	-50	mA
Continuous Output Current		V_{OUT}=0~V_{CCO}	I_{OUT}	±50	mA
Supply Current		I_{CCA} or I_{CCB}	I_{CC} / I_{GND}	±100	mA
Storage Temperature Range			T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. V_{CCO} is the supply voltage associated with the output.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CCA}		1.65		3.6	V
Supply Voltage		V_{CCB}		2.3		5.5	V
Input Voltage		V_{IN}		0		V_{CCI}	V
Output Voltage	A Port	V_{OUT}	V_{CCA}=1.65V~3.6V, V_{CCB}=2.3V~5.5V	0		3.6	V
	B Port			0		5.5	V
High-Level Input Voltage	A Port	V_{IH}	V_{CCA}=1.65V~1.95V, V_{CCB}=2.3V~5.5V	V_{CCI}-0.2		V_{CCI}	V
			V_{CCA}=2.3V~3.6V, V_{CCB}=2.3V~5.5V	V_{CCI}-0.4		V_{CCI}	V
	B Port		V_{CCA}=1.65V~3.6V, V_{CCB}=2.3V~5.5V	V_{CCI}-0.4		V_{CCI}	V
	OE Input			0.65 xV_{CCA}		5.5	V
Low-Level Input Voltage	A or B Port	V_{IL}	V_{CCA}=1.65V~3.6V, V_{CCB}=2.3V~5.5V	0		0.15	V
	OE Input			0		0.35 xV_{CCA}	V
Input Transition Rise or Fall Rate	A or B Port	Δt/Δv	V_{CCA}=1.65V~3.6V, V_{CCB}=2.3V~5.5V			10	ns/V
	OE Input					10	ns/V
Operating Temperature		T_A		-40		+125	°C

Notes: 1. The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.
2. V_{CCA} must be less than or equal to V_{CCB}.

■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
High-Level Output Voltage	A or B Port	V_{OH}	V_{CCA}=1.65V~3.6V, V_{CCB}=2.3V~5.5V, I_{OH}=-20μA		0.67 ×V_{CCO}			V
Low-Level Output Voltage	A or B Port	V_{OL}	V_{CCA}=1.65V~3.6V, V_{CCB}=2.3V~5.5V, I_{OL}=1mA V_{IN}≤0.5V				0.4	V
Input Leakage Current	OE Input	$I_{I(LEAK)}$	V_{IN}=0~3.6V, V_{CCA}=1.65V~3.6V, V_{CCB}=2.3V~5.5V				±12	μA
Power OFF Leakage Current	A Port	I_{OFF}	V_{IN} or V_{OUT}=0~3.6V, V_{CCA}=0V, V_{CCB}=0V~5.5V				±12	μA
	B Port		V_{IN} or V_{OUT}=0~3.6V, V_{CCA}=0V~3.6V, V_{CCB}=0V				±12	μA
Output OFF-State Current	A or B Port	I_{OZ}	V_{OUT}=0V or V_{CCO}, V_{CCA}=1.65V~3.6V, V_{CCB}=2.3V~5.5V				±12	μA
Quiescent Supply Current		I_{CCA}	V_{IN}=0V or V_{CCI} I_{OUT}=0A	V_{CCA}=1.65V~3.6V V_{CCB}=2.3V~5.5V			15	μA
				V_{CCA}=3.6V, V_{CCB}=0V			15	μA
				V_{CCA}=0V, V_{CCB}=5.5V			-8	μA
		I_{CCB}		V_{CCA}=1.65V~3.6V V_{CCB}=2.3V~5.5V			30	μA
				V_{CCA}=3.6V, V_{CCB}=0V			-5	μA
				V_{CCA}=0V, V_{CCB}=5.5V			6	μA
		I_{CCA}+I_{CCB}		V_{CCA}=1.65V~3.6V V_{CCB}=2.3V~5.5V			45	μA
Input Capacitance	OE Input	C_{IN}	V_{CCA}=3.3V, V_{CCB}=3.3V			2		pF
Output Capacitance	A Port	C_{IO}				4		pF
	B Port					7		pF
	A or B Port		V_{CCA}=3.3V, V_{CCB}=3.3V			9		pF

Notes: 1. V_{CCI} is the supply voltage associated with the input port.
2. V_{CCO} is the supply voltage associated with the output port.

■ SWITCHING CHARACTERISTICS (T_A=25°C , unless otherwise specified)

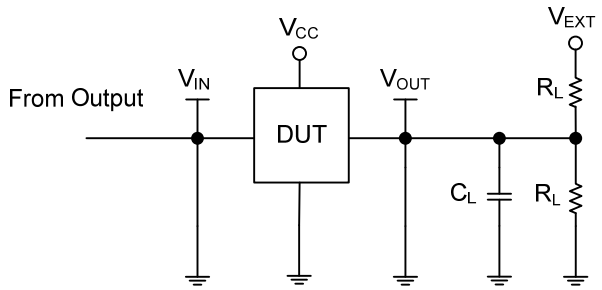
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay From Input (A) to Output (B)	t_{PHL}	V_{CCA}=1.8V±0.15V	V_{CCB}=2.5V±0.2V			5.8	ns
			V_{CCB}=3.3V±0.3V			5.9	ns
			V_{CCB}=5V±0.5V			7.3	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V			4.0	ns
			V_{CCB}=3.3V±0.3V			4.2	ns
			V_{CCB}=5V±0.5V			4.3	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V			3.0	ns
			V_{CCB}=5V±0.5V			3.9	ns
Propagation Delay From Input (B) to Output (A)		V_{CCA}=1.8V±0.15V	V_{CCB}=2.5V±0.2V			5.5	ns
			V_{CCB}=3.3V±0.3V			5.7	ns
			V_{CCB}=5V±0.5V			5.9	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V			3.8	ns
			V_{CCB}=3.3V±0.3V			4.5	ns
			V_{CCB}=5V±0.5V			5.4	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V			3.2	ns
			V_{CCB}=5V±0.5V			4.2	ns
Propagation Delay From Input (A) to Output (B)	t_{PLH}	V_{CCA}=1.8V±0.15V	V_{CCB}=2.5V±0.2V			8.5	ns
			V_{CCB}=3.3V±0.3V			8.5	ns
			V_{CCB}=5V±0.5V			8.8	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V			4.4	ns
			V_{CCB}=3.3V±0.3V			5.2	ns
			V_{CCB}=5V±0.5V			5.5	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V			5.3	ns
			V_{CCB}=5V±0.5V			5.5	ns
Propagation Delay From Input (B) to Output (A)		V_{CCA}=1.8V±0.15V	V_{CCB}=2.5V±0.2V			6.7	ns
			V_{CCB}=3.3V±0.3V			5.7	ns
			V_{CCB}=5V±0.5V			3.1	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V			3.2	ns
			V_{CCB}=3.3V±0.3V			2.0	ns
			V_{CCB}=5V±0.5V			1.9	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V			3.2	ns
			V_{CCB}=5V±0.5V			3.3	ns
Enable Time From Input (OE) to Output (A or B)	t_{en}	V_{CCA}=1.8V±0.15V	V_{CCB}=2.5V±0.2V			250	ns
			V_{CCB}=3.3V±0.3V			200	ns
			V_{CCB}=5V±0.5V			200	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V			200	ns
			V_{CCB}=3.3V±0.3V			200	ns
			V_{CCB}=5V±0.5V			200	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V			200	ns
			V_{CCB}=5V±0.5V			200	ns
Disable Time From Input (OE) to Output (A or B)	t_{dis}	V_{CCA}=1.8V±0.15V	V_{CCB}=2.5V±0.2V			45	ns
			V_{CCB}=3.3V±0.3V			45	ns
			V_{CCB}=5V±0.5V			45	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V			45	ns
			V_{CCB}=3.3V±0.3V			45	ns
			V_{CCB}=5V±0.5V			45	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V			45	ns
			V_{CCB}=5V±0.5V			45	ns

■ SWITCHING CHARACTERISTICS (Cont.)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output Transition Time	A Port	t_{THL}	V_{CCA}=1.8V±0.15V	V_{CCB}=2.5V±0.2V	2.0		7.4	ns
				V_{CCB}=3.3V±0.3V	1.9		7.5	ns
				V_{CCB}=5V±0.5V	1.7		16.7	ns
			V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V	1.9		7.2	ns
				V_{CCB}=3.3V±0.3V	1.9		6.9	ns
				V_{CCB}=5V±0.5V	1.8		6.7	ns
			V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V	2.0		6.8	ns
				V_{CCB}=5V±0.5V	1.9		6.3	ns
Output Transition Time	B Port		V_{CCA}=1.8V±0.15V	V_{CCB}=2.5V±0.2V	2.9		9.5	ns
				V_{CCB}=3.3V±0.3V	2.8		9.4	ns
				V_{CCB}=5V±0.5V	2.8		12.5	ns
			V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V	2.2		9.8	ns
				V_{CCB}=3.3V±0.3V	2.4		8.4	ns
				V_{CCB}=5V±0.5V	2.6		8.3	ns
			V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V	2.3		9.3	ns
				V_{CCB}=5V±0.5V	2.4		9.5	ns
Output Transition Time	A Port	t_{TLH}	V_{CCA}=1.8V±0.15V	V_{CCB}=2.5V±0.2V	3.2		11.9	ns
				V_{CCB}=3.3V±0.3V	2.3		11.7	ns
				V_{CCB}=5V±0.5V	1.8		9.5	ns
			V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V	2.8		9.3	ns
				V_{CCB}=3.3V±0.3V	2.6		8.3	ns
				V_{CCB}=5V±0.5V	1.8		7.8	ns
			V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V	2.3		7.0	ns
				V_{CCB}=5V±0.5V	1.9		7.4	ns
Output Transition Time	B Port		V_{CCA}=1.8V±0.15V	V_{CCB}=2.5V±0.2V	3.3		13.5	ns
				V_{CCB}=3.3V±0.3V	2.7		11.4	ns
				V_{CCB}=5V±0.5V	2.7		9.5	ns
			V_{CCA}=2.5V±0.2V	V_{CCB}=2.5V±0.2V	3.2		10.4	ns
				V_{CCB}=3.3V±0.3V	2.9		9.7	ns
				V_{CCB}=5V±0.5V	2.4		8.3	ns
			V_{CCA}=3.3V±0.3V	V_{CCB}=3.3V±0.3V	2.5		8.0	ns
				V_{CCB}=5V±0.5V	2.1		9.3	ns
Data Rate		f_{data}	V_{CCA}=1.65~3.6V V_{CCB}=2.3V~5.5V				50	Mbps
Pulse Duration	Data Inputs	t_w	V_{CCA}=1.65~3.6V V_{CCB}=2.3V~5.5V		20			ns

Note: Delay between OE going LOW and when the outputs are actually disabled.

■ TEST CIRCUIT AND WAVEFORMS



Notes: R_L=Load resistance.
C_L=Load capacitance including jig and probe capacitance.
V_{EXT}=External voltage for measuring switching times.

Table 1. Measurement Points

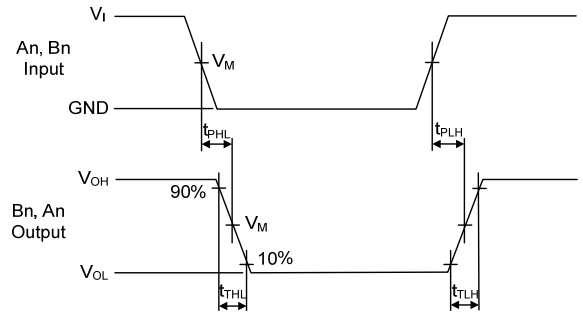
Supply Voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.8V±0.15V	0.5×V_{CCI}	0.5×V_{CCO}	V_{OL}+0.15V	V_{OH}－0.15V
2.5V±0.2V	0.5×V_{CCI}	0.5×V_{CCO}	V_{OL}+0.15V	V_{OH}－0.15V
3.3V±0.3V	0.5×V_{CCI}	0.5×V_{CCO}	V_{OL}+0.3V	V_{OH}－0.3V
5V±0.5V	0.5×V_{CCI}	0.5×V_{CCO}	V_{OL}+0.3V	V_{OH}－0.3V

Table 2. Test Data

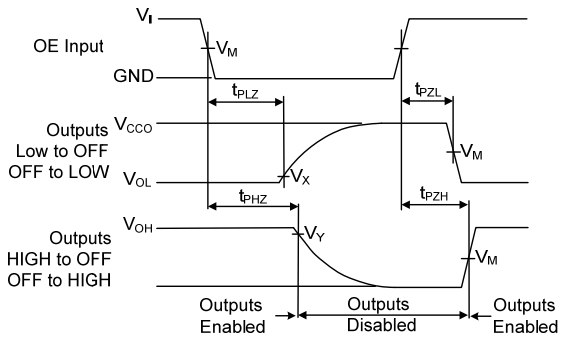
Supply Voltage		Input		Load		V_{EXT}		
V_{CCA}	V_{CCA}	V_I	Δt/Δv	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65V~3.6V	2.3V~5.5V	V_{CCI}	≤1.0 ns/V	15pF	50kΩ, 1MΩ	Open	Open	2xV_{CCO}

Notes: 1. V_{CCI} is the supply voltage associated with the input.
2. For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L=1MΩ; for measuring enable and disable times, R_L=50kΩ.
3. V_{CCO} is the supply voltage associated with the output

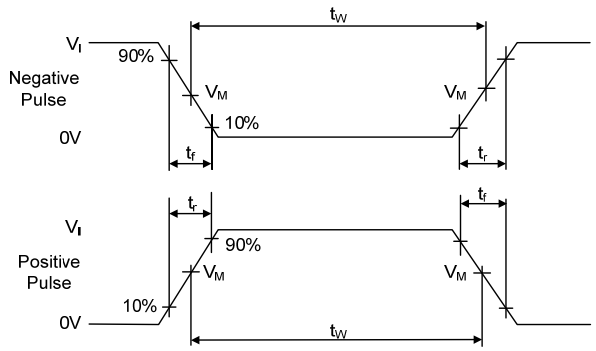
■ TEST CIRCUIT AND WAVEFORMS (Cont.)



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES



TEST SWITCHING TIMES

Notes: 1. V_{CCI} is the supply voltage associated with the input V_{CCO} is the supply voltage associated with the output.

2. All input pulses are supplied by generators having the following characteristics: PRR=10MHz for measuring enable and disable times, Z_O=50kΩ, dv/dt ≥ 1V/ns.

■ APPLICATION INFORMATION

Architecture

The architecture of the **UNTS0104** is shown in Figure 1. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

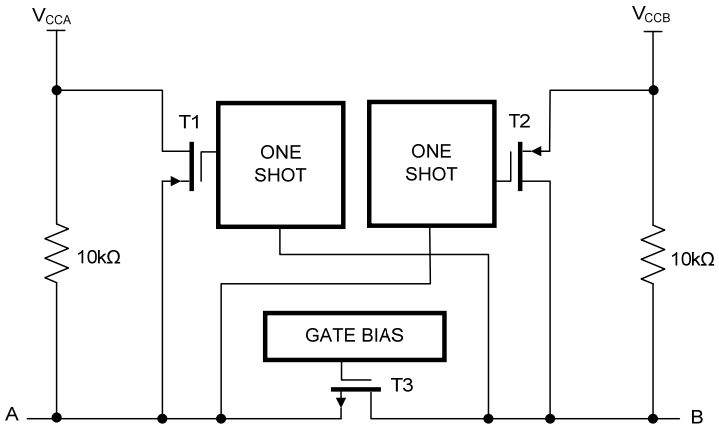


Figure 1. Architecture of I/O Cell (One Channel)

The **UNTS0104** is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the V_{CC} level of the low-voltage side. During a LOW-to-HIGH transition the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2) bypassing the 10kΩ pull-up resistors and increasing current drive capability. The one-shot is activated once the input transition reaches approximately $V_{CCI}/2$; it is de-activated approximately 50 ns after the output reaches $V_{CCO}/2$. During the acceleration time the driver output resistance is between approximately 50Ω and 70Ω. To avoid signal contention and minimize dynamic I_{CC}, the user should wait for the one-shot circuit to turn-off before applying a signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

Input Driver Requirements

As the **UNTS0104** is a switch type translator, properties of the input driver directly effect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system; the max data rate, HIGH-to-LOW output transition time (t_{THL}) and propagation delay (t_{PHL}) are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the datasheet assume a driver with output impedance below 50Ω is used.

Output load considerations

The maximum lumped capacitive load that can be driven is dependant upon the one-shot pulse duration. In cases with very heavy capacitive loading there is a risk that the output will not reach the positive rail within the one-shot pulse duration. To avoid excessive capacitive loading and to ensure correct triggering of the one-shot it's recommended to use short trace lengths and low capacitance connectors on **UNTS0104** PCB layouts. To ensure low impedance termination and avoid output signal oscillations and one-shot re-triggering, the length of the PCB trace should be such that the round trip delay of any reflection is within the one-shot pulse duration (approximately 50 ns).

Power-up

During operation V_{CCA} must never be higher than V_{CCB}, however during power-up $V_{CCA} \geq V_{CCB}$ does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The **UNTS0104** includes circuitry that disables all output ports when either V_{CCA} or V_{CCB} is switched off.

■ APPLICATION INFORMATION (Cont.)

Enable and disable

An output enable input (OE) is used to disable the device. Setting OE=LOW causes all I/Os to assume the high-impedance OFF-state. The disable time indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (ten) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Pull-up or pull-down resistors on I/Os lines

Each A port I/O has an internal 10kΩ pull-up resistor to V_{CCA}, and each B port I/O has an internal 10kΩ pull-up resistor to V_{CCB}. If a smaller value of pull-up resistor is required, an external resistor must be added parallel to the internal 10kΩ , this will effect the V_{OL} level. When OE goes LOW the internal pull-ups of the **UNTS0104** are disabled.

■ TYPICAL APPLICATION CIRCUIT