



## ULD2003

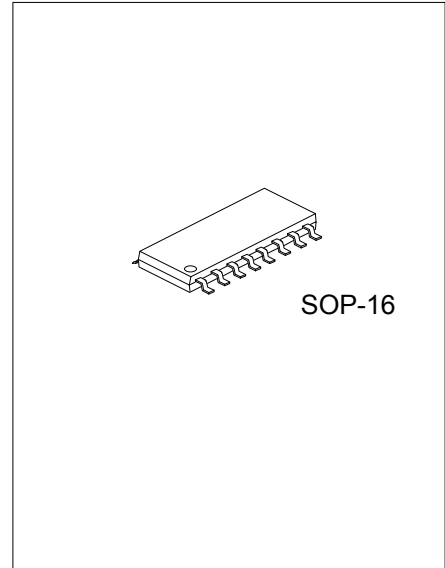
Advance

CMOS IC

### 7 CHANNEL SINK TYPE DMOS TRANSISTOR ARRAY

#### DESCRIPTION

The UTC **ULD2003** is DMOS transistor array with 7 circuits. It has a clamp diode for switching inductive loads built-in in each output. Please be careful about thermal conditions during use.



#### FEATURES

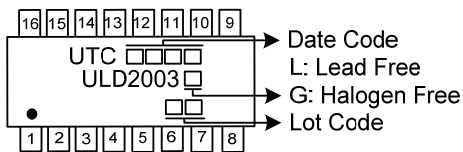
- \* 7 circuits built-in
- \* High voltage:  $V_{OUT} = 50V$  (MAX)
- \* High current:  $I_{OUT} = 500mA/ch$  (MAX)
- \* Input voltage(output on): 2.5V (MIN)
- \* Input voltage(output off): 0.6V (MAX)

#### ORDERING INFORMATION

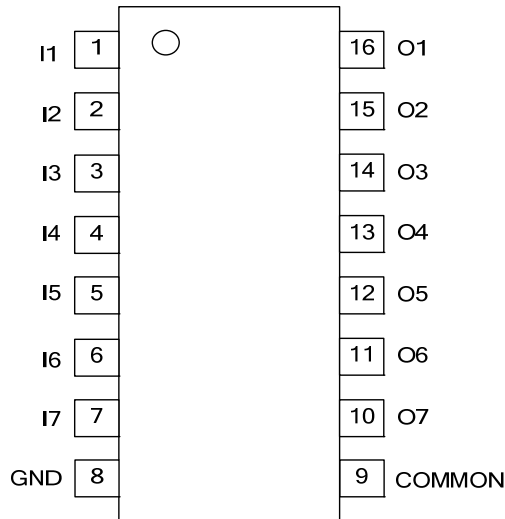
Ordering Number		Package	Packing
Lead Free	Halogen Free		
ULD2003L-S16-R	ULD2003G-S16-R	SOP-16	Tape Reel

<p>ULD2003G-S16-R</p> <ul style="list-style-type: none"> <li>(1) Packing Type</li> <li>(2) Package Type</li> <li>(3) Green Package</li> </ul>	<ul style="list-style-type: none"> <li>(1) R: Tape Reel</li> <li>(2) S16: SOP-16</li> <li>(3) G: Halogen Free and Lead Free, L: Lead Free</li> </ul>
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#### MARKING



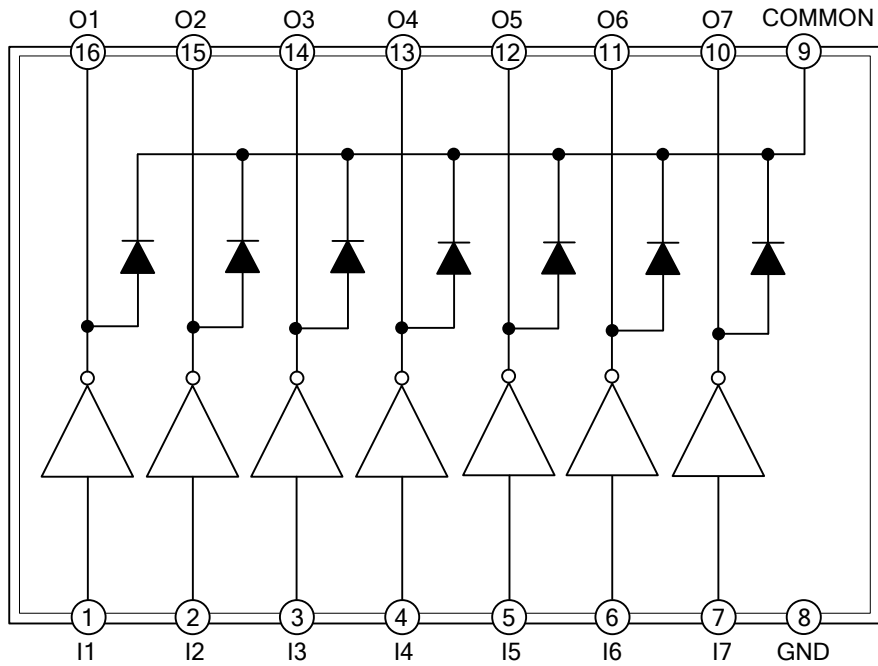
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	I1	1 Channel Input pin
2	I2	2 Channel Input pin
3	I3	3 Channel Input pin
4	I4	4 Channel Input pin
5	I5	5 Channel Input pin
6	I6	6 Channel Input pin
7	I7	7 Channel Input pin
8	GND	GND pin
9	COMMON	Common pin
10	Q7	7 Channel Output pin
11	Q6	6 Channel Output pin
12	Q5	5 Channel Output pin
13	Q4	4 Channel Output pin
14	Q3	3 Channel Output pin
15	Q2	2 Channel Output pin
16	Q1	1 Channel Output pin

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T<sub>A</sub>=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Output Voltage	V <sub>OUT</sub>	50	V
COMMON Pin Voltage	V <sub>COM</sub>	-0.5 ~ 50	V
Output Current	I <sub>OUT</sub>	500	mA/ch
Input Voltage	V <sub>IN</sub>	-0.5 ~ 30	V
Clamp Diode Reverse Voltage	V <sub>R</sub>	50	V
Clamp Diode Forward Current	I <sub>F</sub>	500	mA
Power Dissipation (Note 1)	P <sub>D</sub>	1.25	W
Operating Temperature	T <sub>OPR</sub>	-40 ~ +85	°C
Storage Temperature	T <sub>STG</sub>	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ OPERATING RANGES (T<sub>A</sub>=-40~+85°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Output Voltage	V <sub>OUT</sub>				50	V	
COMMON Pin Voltage	V <sub>COM</sub>		0		50	V	
Output Current (Note 1)	I <sub>OUT</sub>	1 Circuits ON, T <sub>a</sub> =25°C	0		400	mA/ch	
		t <sub>PW</sub> =25ms 7 Circuits ON T <sub>A</sub> =85°C		Duty = 10%	0	390	mA/ch
		T <sub>J</sub> =120°C		Duty = 50%	0	170	mA/ch
Input Voltage (Output On)	V <sub>IN(ON)</sub>	I <sub>OUT</sub> =100mA or Upper, V <sub>OUT</sub> =2V	2.5		25	V	
Input Voltage (Output Off)	V <sub>IN(OFF)</sub>	I <sub>OUT</sub> =100μA or Less, V <sub>OUT</sub> =2V	0		0.6	V	
Clamp Diode Forward Current	I <sub>F</sub>				400	mA	

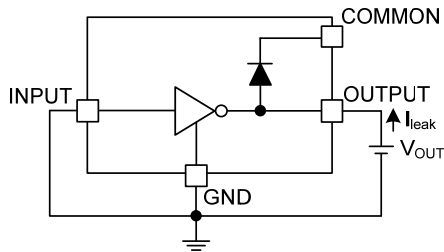
Note: On PCB (JEDEC 2s2p).

■ ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

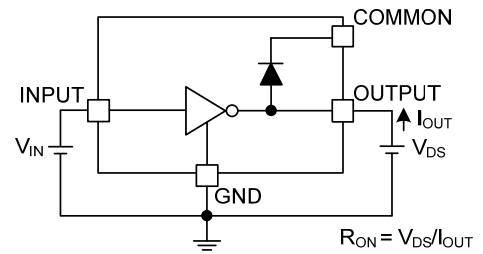
PARAMETER	SYMBOL	Test Circuit	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Leakage Current	I <sub>leak</sub>	1	V <sub>OUT</sub> =50V, T <sub>A</sub> =85°C, V <sub>IN</sub> =0V			1.0	μA
Output Voltage (Output ON-Resistance)	V <sub>DS</sub> (R <sub>ON</sub> )	2	I <sub>OUT</sub> =350mA, V <sub>IN</sub> =5.0V		0.7 (2.0)	1.14 (3.25)	V (Ω)
			I <sub>OUT</sub> =200mA, V <sub>IN</sub> =5.0V		0.4 (2.0)	0.65 (3.25)	V (Ω)
			I <sub>OUT</sub> =100mA, V <sub>IN</sub> =5.0V		0.2 (2.0)	0.325 (3.25)	V (Ω)
Input Current (Output On)	I <sub>IN(ON)</sub>	3	V <sub>IN</sub> =2.5V			0.1	mA
Input Current (Output Off)	I <sub>IN(OFF)</sub>	4	V <sub>IN</sub> =0V, T <sub>A</sub> =85°C			1.0	μA
Input Voltage (Output On)	V <sub>IN(ON)</sub>	5	I <sub>OUT</sub> =100mA, V <sub>OUT</sub> =2V			2.5	V
Clamp Diode Reverse Current	I <sub>R</sub>	6	V <sub>R</sub> =50V, T <sub>A</sub> =85°C			1.0	μA
Clamp Diode Forward Voltage	V <sub>F</sub>	7	I <sub>F</sub> =350mA			2.0	V
Turn-On Delay	t <sub>ON</sub>	8	V <sub>OUT</sub> =50V, R <sub>L</sub> =125Ω, C <sub>L</sub> =15pF		0.5		μs
Turn-Off Delay	t <sub>OFF</sub>				0.1		μs

■ TEST CIRCUIT

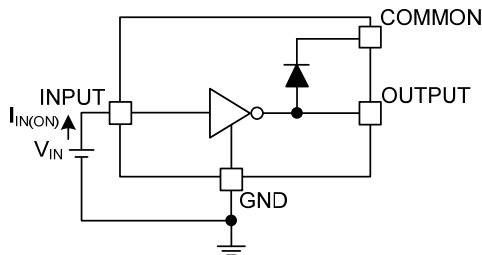
1.  $I_{leak}$



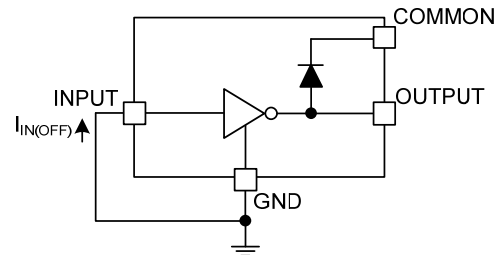
2.  $V_{DS} (R_{ON})$



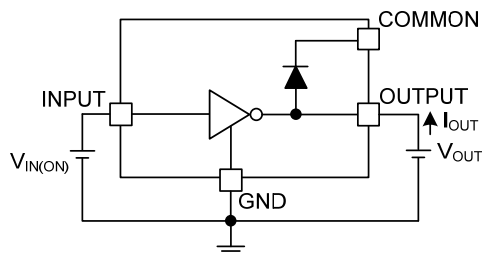
3.  $I_{IN(ON)}$



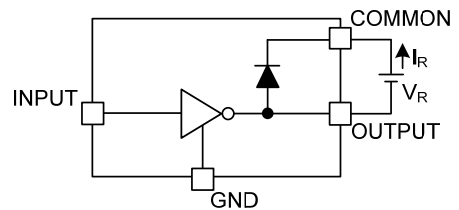
4.  $I_{IN(OFF)}$



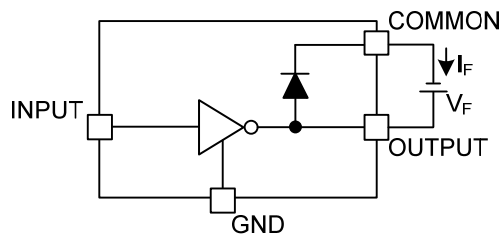
5.  $V_{IN(ON)}$



6.  $I_R$



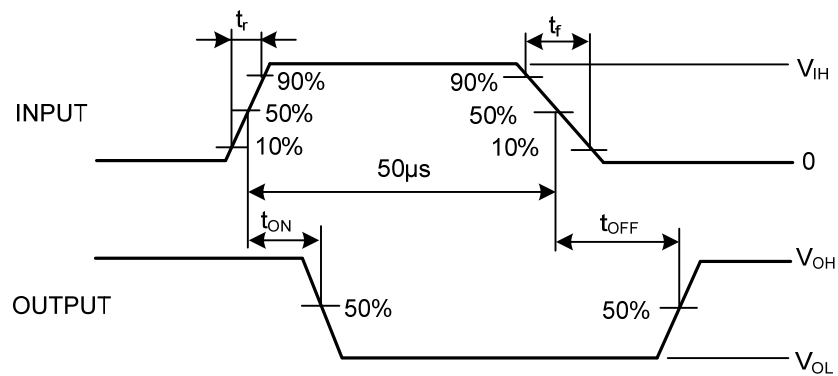
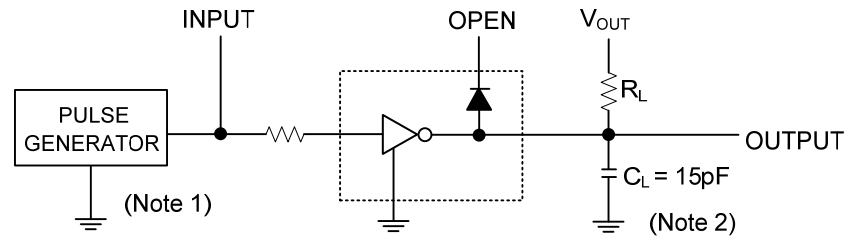
7.  $V_F$



Test circuit may be simplified for explanatory purpose.

■ TEST CIRCUIT (Cont.)

8.  $t_{ON}$ ,  $t_{OFF}$



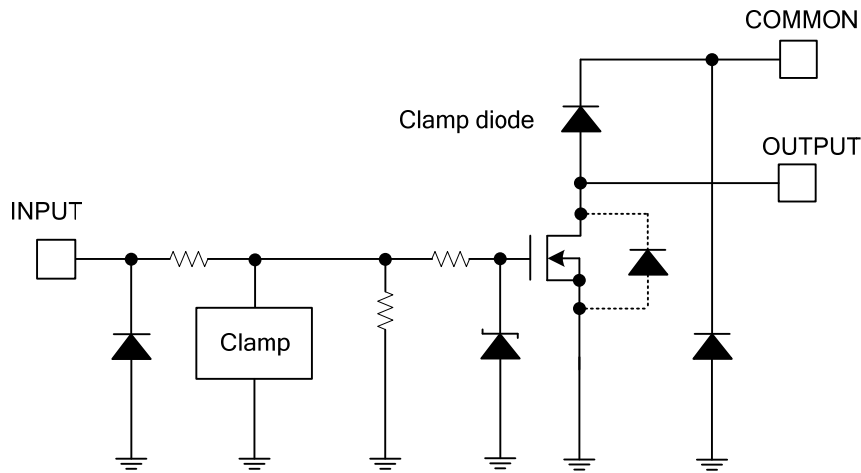
Note 1: Pulse width 50µs, Duty cycle 10%  
 Output impedance 50Ω,  $t_r \leq 5ns$ ,  $t_f \leq 10ns$   
 Please refer to the following table for the  $V_{IH}$  condition.

Product	$V_{IH}$
ULD2003	5.0V

2.  $C_L$  includes the probe and the test board capacitance.

Test circuit and timing chart may be simplified for explanatory purpose.

■ EQUIVALENT CIRCUIT (EACH DRIVER)



Equivalent circuit may be simplified for explanatory purpose.

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