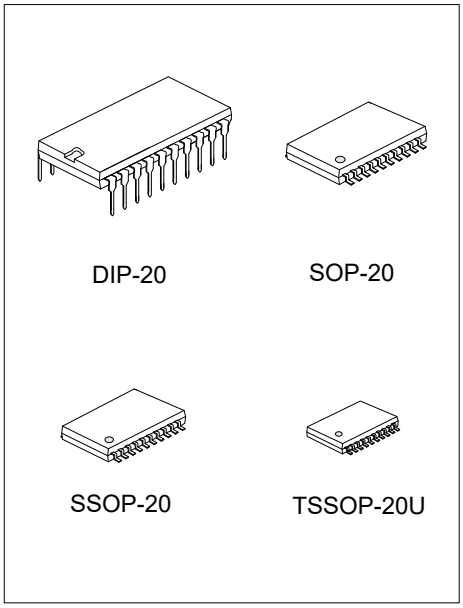
U74AHCT273

CMOS IC

OCTAL D-TYPE FLIP-FLOPS WITH CLEAR



■ DESCRIPTION

The **U74AHCT273** devices are positive-edge-triggered D-type flip-flops with a direct active low clear ($\overline{CLR}$) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not related directly to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

■ FEATURES

* Operating Voltage Range of 4.5V to 5.5V
* Inputs are TTL-Voltage Compatible
* ±8mA Output Drive at 5V
* Contain Eight Flip-Flops With Single-Rail Outputs
* Direct Clear Input
* Individual Data Input to Each Flip-Flop

■ ORDERING INFORMATION

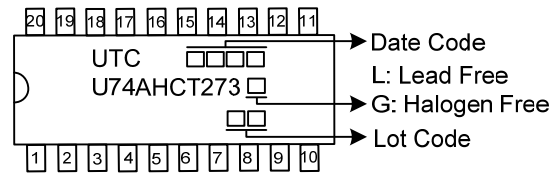
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHCT273L-D20-T	U74AHCT273G-D20-T	DIP-20	Tube
U74AHCT273L-S20-R	U74AHCT273G-S20-R	SOP-20	Tape Reel
U74AHCT273L-R20-R	U74AHCT273G-R20-R	SSOP-20	Tape Reel
U74AHCT273L-ULA-R	U74AHCT273G-ULA-R	TSSOP-20U	Tape Reel

U74AHCT273G-D20-T
(1)Packing Type
(2)Package Type
(3)Green Package

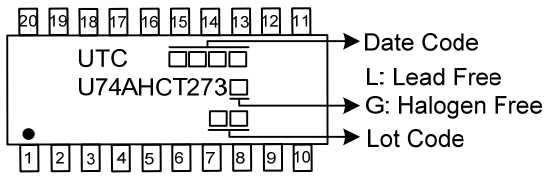
(1) T: Tube, R: Tape Reel
(2) D20: DIP-20, S20: SOP-20, R20: SSOP-20
ULA: TSSOP-20U
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

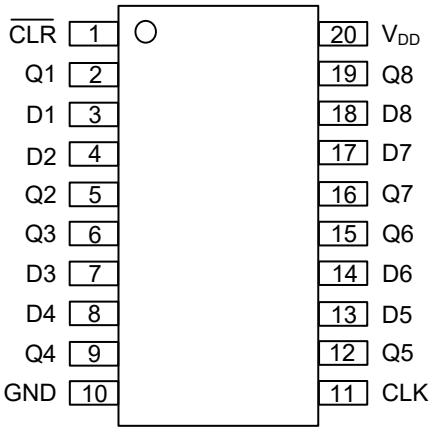
DIP-20



SOP-20 / SSOP-20 / TSSOP-20U



■ PIN CONFIGURATION

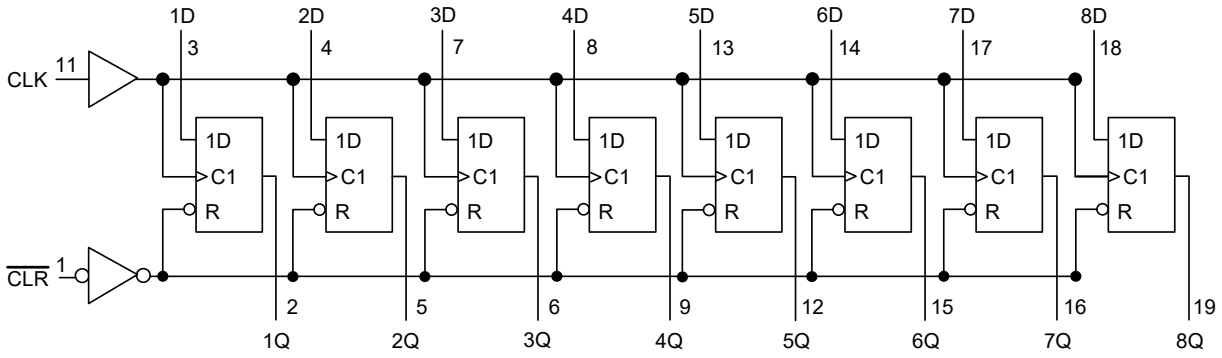


■ FUNCTION TABLE

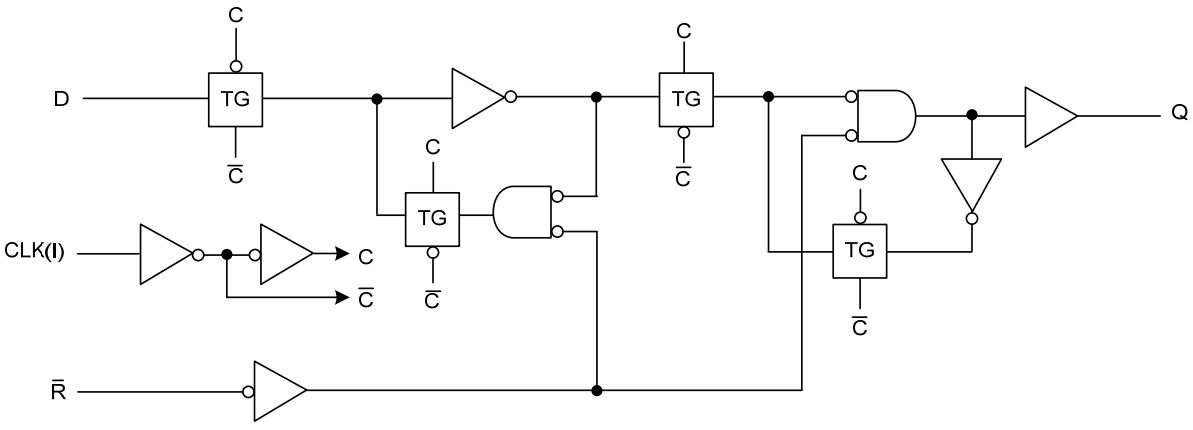
INPUTS			OUTPUT
$\overline{CLR}$	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = High voltage level ; L = Low voltage level ; X = Don't care

■ FUNCTIONAL BLOCK DIAGRAM



■ LOGIC DIAGRAM, EACH FLIP-FLOP (POSITIVE LOGIC)



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 7	V
Input Voltage Range	V_I		-0.5 ~ 7	V
Output Voltage Range	V_O		-0.5 ~ V_{CC} +0.5	V
Continuous Output Current	I_{OUT}	V_{OUT}=0 ~ V_{CC}	±25	mA
Input Clamp Current	I_{IK}	V_{IN}<0 or V_{IN}<V_{CC}	±20	mA
Output Clamp Current	I_{OK}	V_{IN}<0 or V_{OUT}>V_{CC}	±20	mA
Continuous Current Through V_{CC} or GND			±75	mA
Operating Temperature	T_A		-40 ~ +125	°C
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5	5	5.5	V
High-Level Input Voltage	V_{IH}	V_{CC}=4.5~5.5V	2			V
Low-Level Input Voltage	V_{IL}	V_{CC}=4.5~5.5V			0.8	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
High-Level output current	I_{OH}		-8			mA
Low-Level output current	I_{OL}				8	mA

■ ELECTRICAL CHARACTERISTICS (T_A =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	V_{CC}=4.5V, I_{OH}=-50μA	4.4	4.5		V
		V_{CC}=4.5V, I_{OH}=-8mA	3.94			
Low-Level Output Voltage	V_{OL}	V_{CC}=4.5V, I_{OL}=50μA			0.1	V
		V_{CC}=4.5V, I_{OL}=8mA			0.36	
Input Leakage Current	$I_{I(LEAK)}$	V_I=V_{CC} or GND			±0.1	μA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_I=V_{CC} or GND, I_{OUT}=0			4	μA
Additional Quiescent Supply Current (Note)	ΔI_{CC}	V_{CC}=5.5V,One input at 3.4V, Other Inputs at V_{CC} or GND.			1.35	mA
Input Capacitance	C_I	V_{CC}=5V, V_I=V_{CC} or GND		3	10	pF

Note: The increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

■ SWITCHING CHARACTERISTICS (V_{CC}=5V±0.5V, T_A =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum clock pulse frequency	f_{MAX}	C_L=15pF	75	120		MHz
		C_L=50pF	50	75		MHz
Propagation delay from input ($\overline{CLR}$) to output (Q)	t_{PHL}	C_L=15pF		7.5	10	ns
		C_L=50pF		8.5	11	ns
Propagation delay from input (CLK) to output (Q)	t_{PLH}	C_L=15pF		5.5	7.5	ns
		C_L=50pF		6.5	8.5	ns
	t_{PHL}	C_L=15pF		5.8	8.2	ns
		C_L=50pF		6.8	9.2	ns
Propagation delay	$t_{SK(O)}$	C_L=50pF			1	ns

■ TIMING REQUIREMENTS (V_{CC}=5V±0.5V, T_A =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pulse duration	t_W	CLK high or low	5			ns
		$\overline{CLR}$ low	5			ns
Setup time before CLK↑	t_{SU}	Data before CLK ↑	5			ns
		$\overline{CLR}$ before CLK ↑	3			ns
Hold time ,data after CLK↑	t_h		1			ns

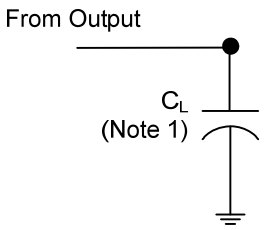
■ NOISE CHARACTERISTICS (V_{CC}=5V, C_L=50pF, T_A =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$			7.6		V
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$			-0.48		V
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$		4.4			V
High-level dynamic input voltage	$V_{IH(D)}$		2			V
Low-level dynamic input voltage	$V_{IL(D)}$				0.8	V

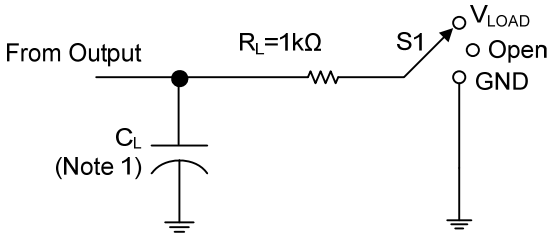
■ OPERATING CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance per flip-flop	C_{PD}	f=1MHz, No load.		27		pF

■ TEST CIRCUIT AND WAVEFORMS

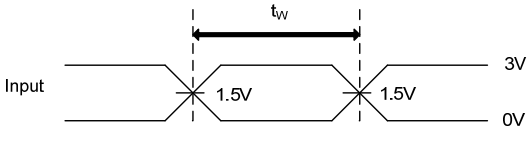


Load Circuit

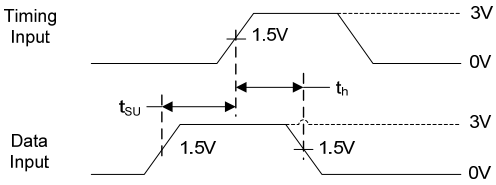


Test Circuit

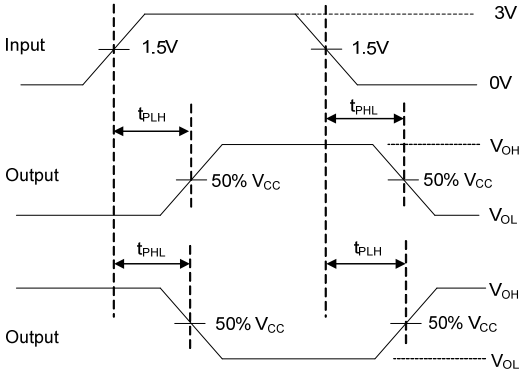
TEST	S1
t_{PLZ}/t_{PZL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



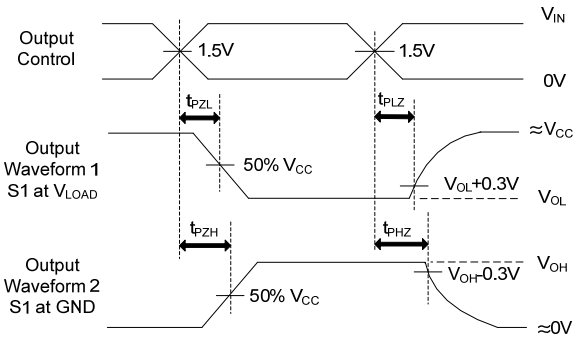
PULSE DURATION



SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR ≤1MHz, Z_O = 50Ω, t_r = 3 ns, t_f = 3 ns.