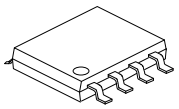
UMD9118

CMOS IC

ELECTRIC TOY DC MOTOR DRIVE CIRCUIT



SOP-8

■ DESCRIPTION

UTC **UMD9118** is an integrated circuit driven by a single channel toy DC motor which is designed for low-voltage operated system. It has H bridge driver and uses the PMOS and NMOS power transistors with low output resistance. Low on-resistance ensures the circuit to consume lower power in operating at a continuous current, and ensures the circuit to operate stably for a long time.

UTC **UMD9118** has on-chip temperature protection function. When load motor with low internal resistance is in locked rotor, UTC **UMD9118** output current will increase momentarily, power dissipation of the circuit will go up sharply, and the chip temperature will soar. But, when the chip temperature exceeds a maximum temperature point (typically 150°C) set by internal temperature protection circuit, the internal circuit will switch off the on-chip power switching transistor of UTC **UMD9118**, and switch off load current, preventing potential safety hazards such as fuming, igniting, etc. Of plastic package caused by over temperature .Only after having confirmed that the circuit has returned to safety temperature, can the on-chip temperature hysteresis circuit be allowed to re-control the circuit.

■ FEATURES

* H bridge driver of internal PMOS/NMOS power switches
* Can realize 4 functions (forward、backward、standby、brake) of load motor
* Low output impedance
* On-chip thermal shut down (TSD) with hysteresis

■ ORDERING INFORMATION

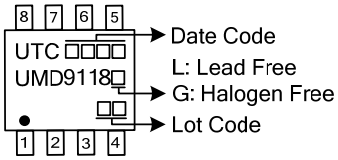
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UMD9118L-S08-R	UMD9118G-S08-R	SOP-8	Tape Reel

UMD9118G-S08-R

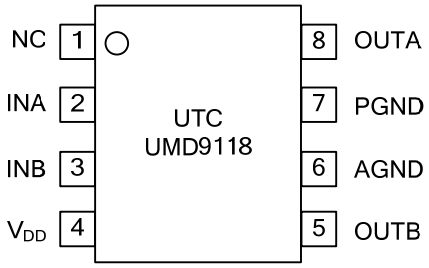
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) S08: SOP-8
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	NC	No connection
2	INA	Logic input INA
3	INB	Logic input INB
4	V_{DD}	Power supply
5	OUTB	Output OUTB
6	AGND	Ground of logic control circuit
7	PGND	Ground of output power transistor
8	OUTA	Output OUTA

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	7	V
Peak Output Current/Channel	I_{OP}	2.5	A
Continuous Output Current/Channel	I_{OC}	1.8	A
Maximum Power Dissipation	P_D	0.67	W
Junction Temperature	T_J	+150	°C
Operational Temperature Range	T_{OPR}	-20 ~ +85	°C
Storage Temperature	T_{STG}	-55 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATIONAL CONDITIONS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Power Supply Voltage	V_{DD}	2.4 ~ 6.5	V
Input Voltage	V_{IN}	0 ~ V_{DD}	V
Output Current	I_{OUT}	-1500 ~ 1500	mA

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	186	°C/W

■ ELECTRICAL CHARACTERISTICS

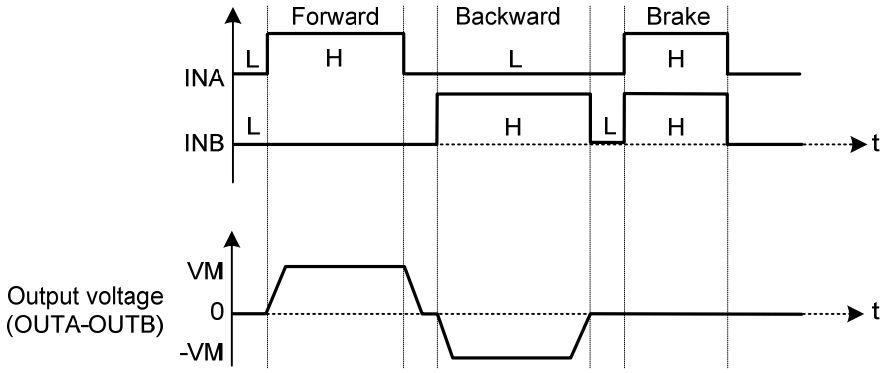
(V_{DD}=3V, R_L=15Ω, C_L=0.1uF, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Working Current						
V_{DD} Standby Current	I_{CCST}	I_{NA}=I_{NB}=L		0	10	μA
V_{DD} Static Supply Current	I_{CC}	I_{NA}=H, I_{NB}=L or I_{NA}=L, I_{NB}=H or I_{NA}=H, I_{NB}=H, I_{OUT}=0A		0.3	1.0	mA
INA/INB						
Input High Level	V_{INH}		0.8×V_{DD}			V
Input Low Level	V_{INL}				0.2×V_{DD}	V
Input High Level Current	I_{INH}	V_{IN}=3V		5	20	uA
Input Low Level Current	I_{INL}	V_{IN}=0V	-1	0		uA
Input the Pull-Down Resistor	R_{IN}			1.5		MΩ
The Power Tube Leads to Internal Resistance						
Output Resistance	R_{ON}	I_O=±200mA		1	1.6	Ω

■ LOGIC TRUTH TABLE

INA	INB	OUTA	OUTB	FUNCTION
L	L	Hi-Z	Hi-Z	Standby (Stop)
H	L	H	L	Forward rotation
L	H	L	H	Backward rotation
H	H	L	L	Brake

■ TYPICAL WAVEFORM



■ TYPICAL APPLICATION CIRCUIT

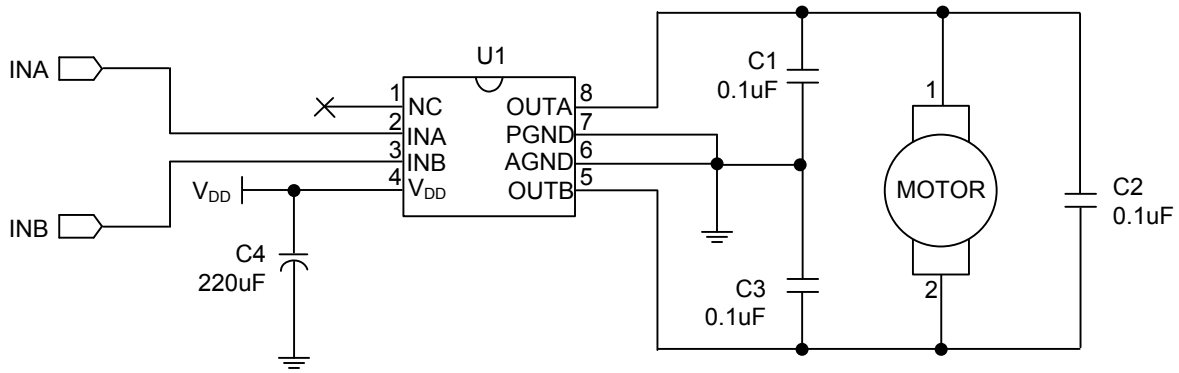


Figure 1. Circuit diagrams for typical application scenarios

Note: A capacitor must be connected between OUTA and OUTB as shown by C2 (0.1uF) in Figure 1.

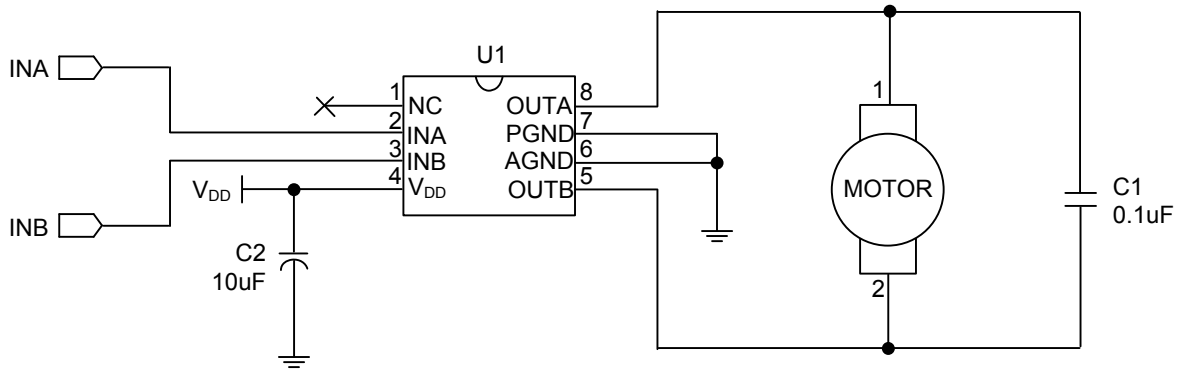


Figure 2. Circuit diagram of low voltage and low voltage interference scheme

Note: A capacitor must be connected between OUTA and OUTB as shown by C1 (0.1uF) in Figure 2.