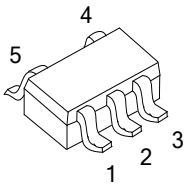
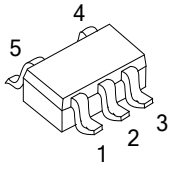
LOW-POWER 2-INPUT NAND GATE WITH OPEN-DRAIN OUTPUT



SOT-23-5
(JEDEC TO-236)



SOT-353

■ DESCRIPTION

The **U74AUP1G38** provides the single 2-input NAND gate with open-drain output. The output of the device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF}.

The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

■ FEATURES

* Wide supply voltage range from 0.8V to 3.6V
* Inputs accept voltages up to 3.6V
* I_{OFF} supports partial-power-down mode
* Low static power consumption; I_{CC}=0.5μA (Max.)
* Optimized for 3.3V Operation

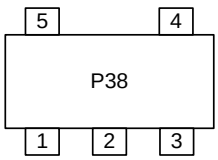
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AUP1G38L-AE5-R	U74AUP1G38G-AE5-R	SOT-23-5	Tape Reel
U74AUP1G38L-AL5-R	U74AUP1G38G-AL5-R	SOT-353	Tape Reel

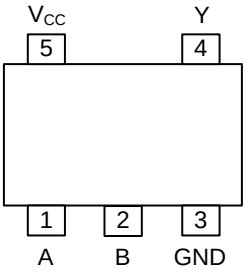
U74AUP1G38G-AE5-R
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) AE5: SOT-23-5, AL5: SOT-353
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

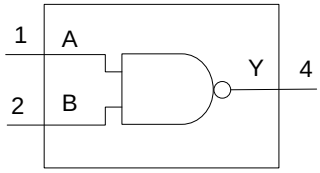


■ FUNCTION TABLE

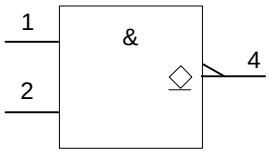
INPUT(A)	INPUT(B)	OUTPUT(Y)
L	L	Z
L	H	Z
H	L	Z
H	H	L

Note: H: HIGH voltage level; L: LOW voltage level; Z: high impedance state.

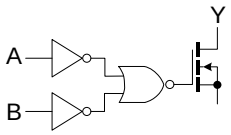
■ LOGIC DIAGRAM (positive logic)



Logic Symbol



IEC Logic Symbol



Logic Diagram

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +4.6	V
Input Voltage	V_{IN}		-0.5 ~ +4.6	V
Output Voltage	V_{OUT}		-0.5 ~ +4.6	V
Continuous V_{CC} or GND Current	I_{CC}		50	mA
Continuous Output Current	I_{OUT}	V_{OUT}=0 ~ V_{CC}	±20	mA
Input Clamp Current	I_{IK}	V_{IN}<0V	-50	mA
Output Clamp Current	I_{OK}	V_{OUT}<0V	-50	mA
Minimum Ground Current	I_{GND}		-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		0.8		3.6	V
Input Voltage	V_{IN}		0		3.6	V
Output Voltage	V_{OUT}		0		3.6	V
Operating Temperature	T_A		-40		+125	°C
Input Transition Rise or Fall Rate	Δt/Δv	V_{CC}=0.8V ~ 3.6V			200	ns/V

■ ELECTRICAL CHARACTERISTICS (T_A =25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	V_{CC}=0.8V		0.7×V_{CC}			V
		V_{CC}=0.9V~1.95V		0.65×V_{CC}			V
		V_{CC}=2.3V~2.7V		1.6			V
		V_{CC}=3.0V~3.6V		2			V
Low-level Input Voltage	V_{IL}	V_{CC}=0.8V				0.3×V_{CC}	V
		V_{CC}=0.9V~1.95V				0.35×V_{CC}	V
		V_{CC}=2.3V~2.7V				0.7	V
		V_{CC}=3.0V~3.6V				0.9	V
Low-Level Output Voltage	V_{OL}	V_{CC}=0.8V~3.6V, I_{OL}=20μA				0.1	V
		V_{CC}=1.1V, I_{OL}=1.1mA				0.3×V_{CC}	V
		V_{CC}=1.4V, I_{OL}=1.7mA				0.31	V
		V_{CC}=1.65V, I_{OL}=1.9mA				0.31	V
		V_{CC}=2.3V	I_{OL}=2.3mA			0.31	V
			I_{OL}=3.1mA			0.44	v
		V_{CC}=3.0V	I_{OL}=2.7mA			0.31	V
			I_{OL}=4.0mA			0.44	v
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=0V~3.6V, V_{IN}=0 ~ 3.6V				±0.1	μA
Output Off State Current	I_{OZ}	V_{CC}=0V~3.6V, V_{OUT}=0 ~ 3.6V V_I= V_{IH} or V_{IL} (and at least one input LOW)				±0.1	μA
Power OFF Leakage Current	I_{OFF}	V_{CC}=0V, V_{IN} or V_{OUT}=0~3.6V				±0.2	μA
Additional Power OFF Leakage Current	ΔI_{OFF}	V_{CC}=0V~0.2V, V_{IN} or V_{OUT}=0V~3.6V				±0.2	μA

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Quiescent Supply Current	I_{CC}	V_{CC}=0.8V~3.6V, I_{OUT}=0 V_{IN}=GND or V_{CC} ~ 3.6V			0.5	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	V_{CC}=3.3V, V_{IN}=V_{CC}-0.6V, I_{OUT}=0A			40	μA
Input Capacitance	C_I	V_{CC}=0~3.6V, V_{IN}=V_{CC} or GND		0.8		pF
Output Capacitance	C_{OUT}	output enabled, V_{CC} =0V, V_{OUT}=GND		1.7		pF
		output disabled, V_{CC} =0V, V_{OUT}=GND		1.1		pF

■ SWITCHING CHARACTERISTICS (T_A =25°C, Input: t_R / t_F=3ns, unless otherwise specified)

(See Fig. 1 and Fig. 2 for test circuit and waveforms.)

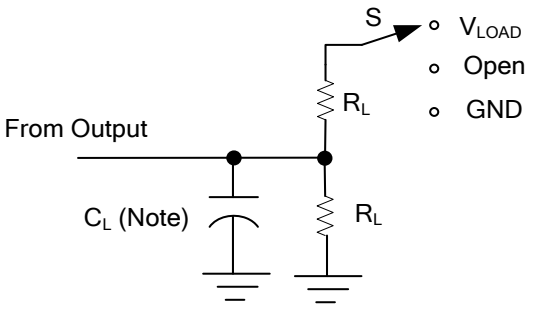
PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation delay from input (A or B) to output (Y)	t_{PD}	C_L=5pF, R_L=5kΩ	V_{CC}=0.8V		13.5		ns
			V_{CC}=1.2V±0.1V	1.9	4.6	10.4	ns
			V_{CC}=1.5V±0.1V	1.5	3.3	6.5	Ns
			V_{CC}=1.8V±0.15V	1.2	2.9	5.1	ns
			V_{CC}=2.5V±0.2V	1.0	2.2	3.8	ns
			V_{CC}=3.3V±0.3V	0.9	2.3	4.0	ns
		C_L=10pF, R_L=5kΩ	V_{CC}=0.8V		16.3		ns
			V_{CC}=1.2V±0.1V	2.3	5.6	12.3	ns
			V_{CC}=1.5V±0.1V	1.8	4.1	7.6	ns
			V_{CC}=1.8V±0.15V	1.6	3.8	6.1	ns
			V_{CC}=2.5V±0.2V	1.4	2.9	4.6	ns
			V_{CC}=3.3V±0.3V	1.3	3.2	5.7	ns
		C_L=15pF, R_L=5kΩ	V_{CC}=0.8V		19		ns
			V_{CC}=1.2V±0.1V	2.6	6.6	14.2	ns
			V_{CC}=1.5V±0.1V	2.1	4.8	8.7	ns
			V_{CC}=1.8V±0.15V	1.9	4.6	7.6	ns
			V_{CC}=2.5V±0.2V	1.6	3.6	5.6	ns
			V_{CC}=3.3V±0.3V	1.6	4.1	7.5	ns
		C_L=30pF, R_L=5kΩ	V_{CC}=0.8V		27		ns
			V_{CC}=1.2V±0.1V	3.6	9.5	19.5	ns
			V_{CC}=1.5V±0.1V	2.9	7.0	11.5	ns
			V_{CC}=1.8V±0.15V	2.6	7.0	12.1	ns
			V_{CC}=2.5V±0.2V	2.4	5.4	8.9	ns
			V_{CC}=3.3V±0.3V	2.3	6.5	12.7	ns

■ OPERATING CHARACTERISTICS

(f=10MHz, V_{IN}=GND to V_{CC}, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	V_{CC}=0.8V		0.6		pF
		V_{CC}=1.1V±0.1V		0.7		pF
		V_{CC}=1.5V±0.1V		0.8		pF
		V_{CC}=1.8V±0.15V		0.9		pF
		V_{CC}=2.5V±0.2V		1.1		pF
		V_{CC}=3.3V±0.3V		1.4		pF

■ TEST CIRCUIT AND WAVEFORMS



TEST	S
t_{PZL} (Note 1)	V_{LOAD}
t_{PLZ} (Note 1)	V_{LOAD}

Note:1. Since this device has open drain outputs, the t_{PLZ} and t_{PZL} is the same as t_{PLH} and t_{PHL}.

Fig. 1 LOAD CIRCUITRY FOR SWITCHING TIMES

Supply Voltage	Input	Output	
V_{CC}	V_M	V_M	$V_\triangle$
0.8V ~ 1.6V	0.5×V_{CC}	0.5×V_{CC}	V_{OL}+0.1V
1.65V ~ 2.7V	0.5×V_{CC}	0.5×V_{CC}	V_{OL}+0.15V
3V ~ 3.6V	0.5×V_{CC}	0.5×V_{CC}	V_{OL}+0.3V

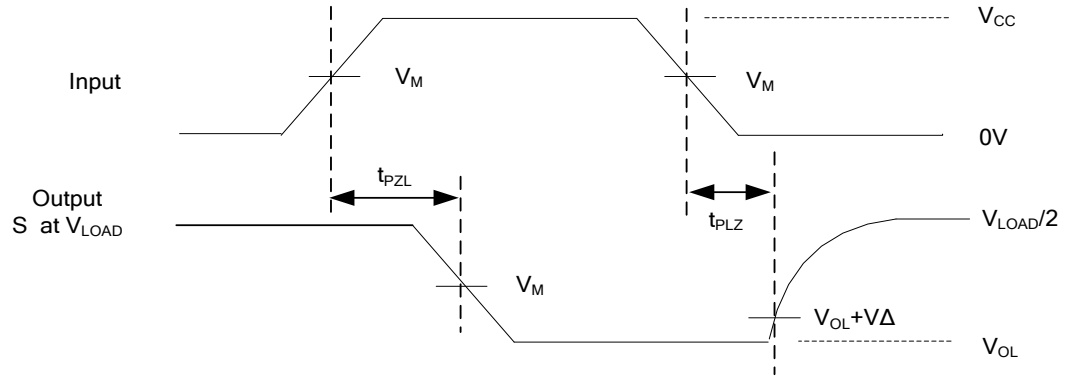


Fig. 2 PROPAGATION DELAY FROM INPUT(A) TO OUTPUT(Y) AND OUTPUT TRANSITION TIME

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω.