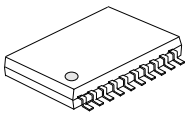
OCTAL D-TYPE FLIP-FLOP; POSITIVE-EDGE TRIGGER; 3-STATE; INVERTING



TSSOP-20

■ DESCRIPTION

The **U74HCT564** is octal D-type flip-flops featuring separate D-type inputs for each flip-flop and inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

■ FEATURES

* 3-state inverting outputs for bus oriented applications
* 8-bit positive-edge triggered register
* Common 3-state output enable input
* Independent register and 3-state buffer operation
* Output capability: bus driver

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT564L-P20-R	U74HCT564G-P20-R	TSSOP-20	Tape Reel

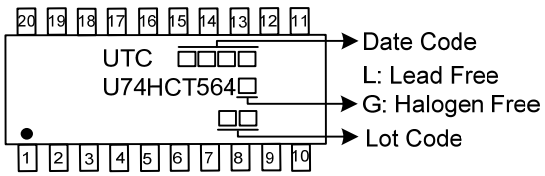
U74HCT564G-P20-R

(1)Packing Type — (1) R: Tape Reel

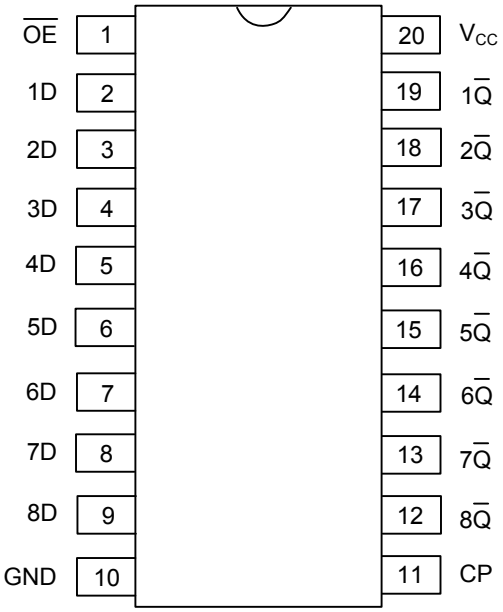
(2)Package Type — (2) P20: TSSOP-20

(3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

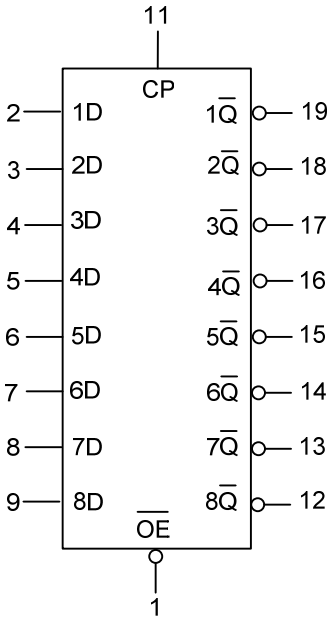


■ FUNCTION TABLE

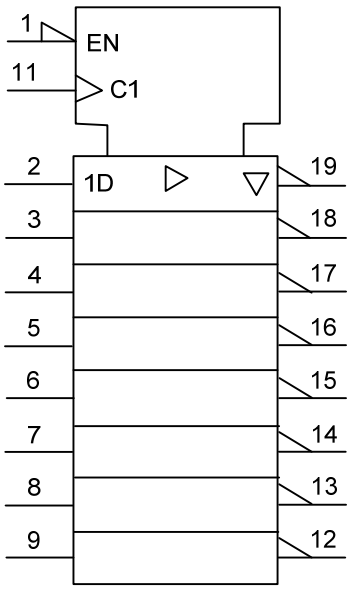
INPUTS			OUTPUT
$\overline{OE}$	CP	D	$\overline{Q}$
L	↑	L	H
L	↑	H	L
L	L	X	No Change
H	X	X	Z

Note: H : HIGH voltage level (Steady State)
L : LOW voltage level(Steady State)
X : Don't Care
Z : high-impedance State
↑ : LOW-to-HIGH clock transition

■ LOGIC SYMBOL AND IEC LOGIC SYMBOL

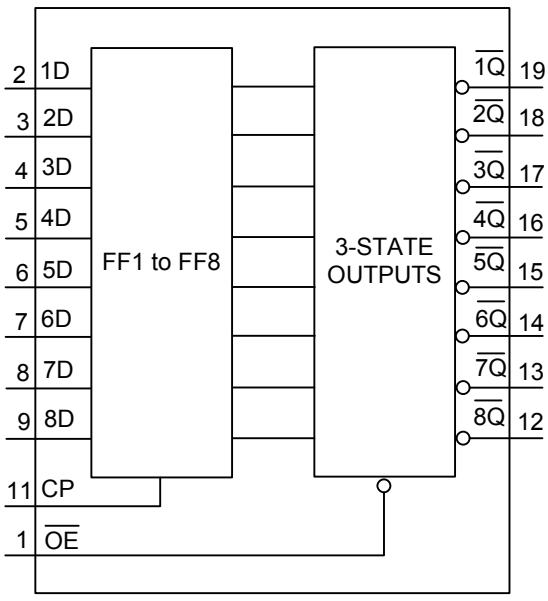


LOGIC SYMBOL

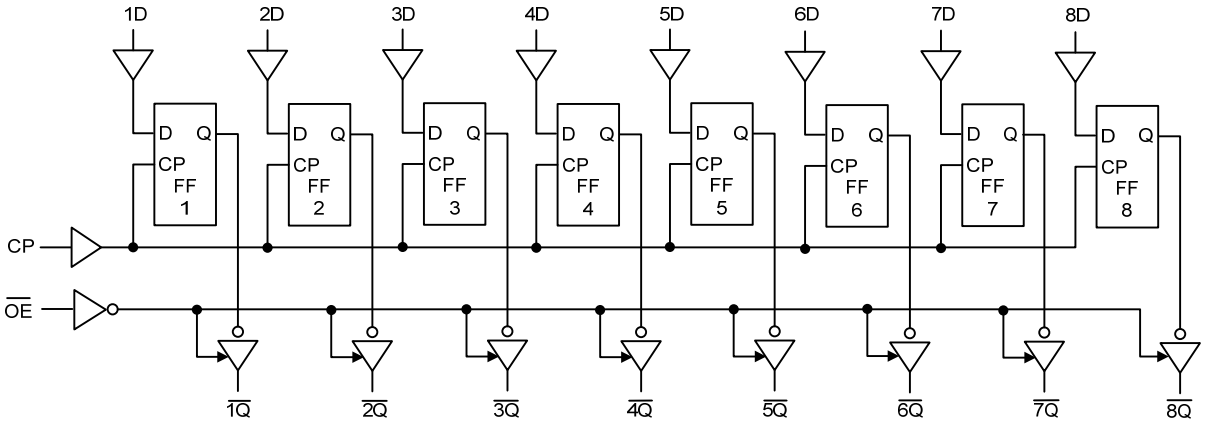


IEC LOGIC SYMBOL

■ FUNCTION DIAGRAM



■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATINGN (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7.0	V
Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
Output Voltage(active mode)	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Clamp Current (V_{iN}<0)	I_{IK}	±20	mA
Output Clamp Current (V_{OUT}<0)	I_{OK}	±20	mA
Output Current	I_{OUT}	±25	mA
V_{CC} or GND Current	I_{CC}	±50	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IN}	0		V_{CC}	V
Output Voltage	V_{OUT}	0		V_{CC}	V
Input Rise and Fall Times	t_R, t_F			500	ns
Operating Temperature	T_{OPR}	-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
High-level Input Voltage	V_{IH}	V_{CC}=4.5V~5.5V		2.0	1.6		V
Lowever Output Voltage	V_{IL}	V_{CC}=4.5V~5.5V			1.2	0.8	V
High-Level Output Voltage, QA-QH	V_{OH}	V_{CC}=4.5V, V_I=V_{IH} or V_{IL}	I_{OH}=-20μA	4.4	4.5		V
			I_{OH}=-6mA	3.98	4.32		V
Low-Level Output Voltage, QA-QH	V_{OL}		I_{OL}=20μA		0	0.1	V
			I_{OL}=6mA		0.16	0.26	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=5.5V, V_{IN}=V_{CC} or GND				±0.1	uA
Output OFF-State Current	I_{OZ}	V_{CC}=5.5V, V_{OUT}=V_{CC} or GND				±0.5	μA
Quiescent Supply Current	I_{CC}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND, I_{OUT}=0				8	μA
Additional Quiescent Supply Current	$\triangle I_{CC}$	V_{CC}=5.5V, one input at V_{CC}-2.1, Other inputs at Vcc or 0.				360	μA
Input Capacitance	C_{IN}	V_{CC}=5.5V, V_{IN}=V_{CC} or GND			3.5		pF

■ TIMING REQUIREMENTS (T_A=25°C, C_L=50pF,unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum clock pulse frequency	f_{MAX}	V_{CC}=4.5V, C_L=50pF	22	36		MHz
Pulse duration width high or Low	t_W		23	14		ns
Setup Time Data before CP	t_{SU}		12	4		ns
Hold Time Data after CP	t_H		5			ns

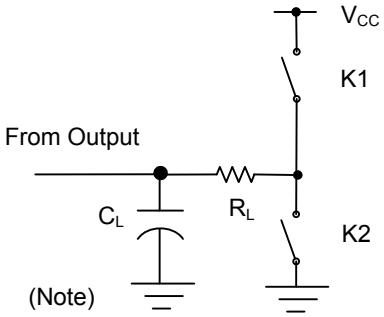
■ DYNAMIC CHARACTERISTICS (T_A=25°C, R_L=1kΩ, unless otherwise specified)

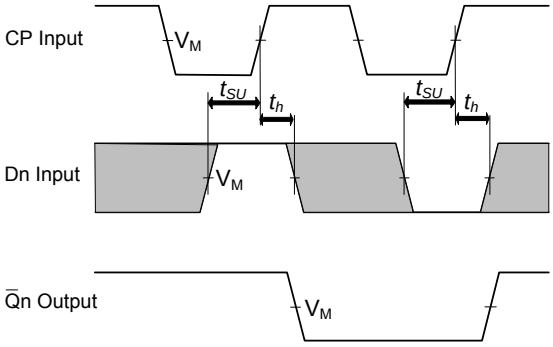
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From Input (CP) to Output ($\overline{Q}$n)	t_{PLH}/t_{PHL}	V_{CC}=4.5V, C_L=50pF		16	35	ns
3-state Output Enable Time From Input ($\overline{OE}$) to Output ($\overline{Q}$n)	t_{PZL}/t_{PZH}			16	30	ns
3-state Output Disable Time From Input ($\overline{OE}$) to Output ($\overline{Q}$n)	t_{PLZ}/t_{PHZ}			18	35	ns
Output Transition Time	t_{THL}/t_{TLH}			5	12	ns

■ OPERATING CHARACTERISTIC (C_L=0, f=10MHz, t_r=t_f=1ns, T_A=25°C, unless otherwise specified)

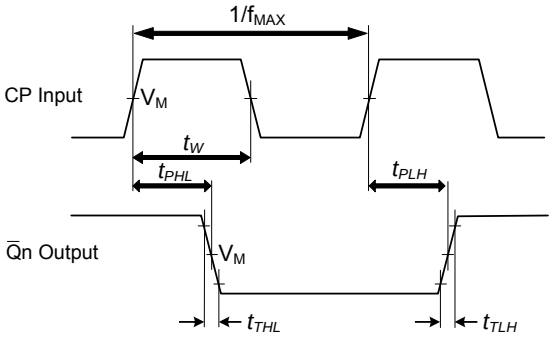
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}			36		pF

■ TEST CIRCUIT AND WAVEFORMS

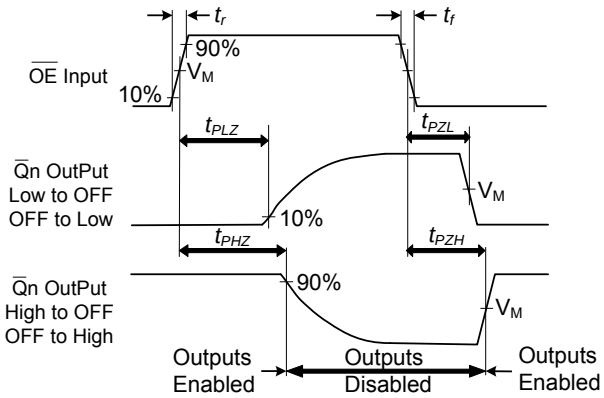




Setup Time and Hold Time



Propagation Delay Times



Enable and Disable Times

Notes：1. C_L includes probe and test-fixture capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤1MHz, Z_O=50Ω, t_r=6ns.